APPLICATION NOTE

ICs for Battery Management

TEA1100 Battery Charger with flyback SMPS current regulator from 12 volt input

Report No: NPO/AN9201

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Keywords
Power Control & Misc.
Battery management
NiCd/NiMH fast charger
TEA1100

Date : 21 oct. 1992
Pages: 23

SUMMARY

A design description is given of a NiCd or NiMH battery charger with the TEA1100 charge and regulation control IC.
The current supply stage is a highly efficient flyback SMPS circuit which includes a current mode slave IC UC3843 and a BUK443-60B power Mosfet switch.
The charger is applicable for a wide range of different voltage batteries and the upper limit is determined by the SMPS design power limitation. A 7.2V battery is maximum with the given charger design.

The charger is outlined for a 12V power source such as a car battery which makes it specially suitable for field use.

The design calculations are extensively given to support redesign on chargers with different requirements.

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1 INTRODUCTION

This paper gives a practical example of a fast charger design for charging , within 1 hour , a NiCd or NiMH battery pack containing up to six , "AA" type cells (500mAhr with NiCd).
This example is a follow up to the charger design for four cells which is described in the TEA1100 applicaton note NPO/AN9102.
The flyback topology applied has the advantage that it provides a large degree of design freedom in charge current magnitude, number of battery cells and input voltage especially. A large number of cells can be charged with a relatively low input voltage (12V). The use of a buck converter, which is popular because of the circuit symplicity, is restricted in the input/output voltage ratio due to the step down principle.

The charge current supply is a discontinuous flyback regulator which is powered from a nominal 12V dc source. It operates according to the current mode principle and is master controlled by the TEA1100 charge management IC. This IC monitors the battery voltage for the battery full event, stabilizes the charge current and determines safe operation in the fast or trickle charge mode.

A full calculation procedure is given for the SMPS power transformer and components design. This simplifies adaptation of the design example to different charger requirements and it might be worthwile to apply the formulae in an electronic spreadsheet.
For the design-in of TEA1100, its time settings and related components can quickly be derived from given graphs.

2 CHARGER SPECIFICATION

- Input voltage range :	9 - 20V dc, 12V nominal
- Output voltage range :	0 - 10.2V.
- Open output voltage :	protection level ≥ 13V.
- Battery type :	7.2V ; 500mAh (6 NiCd cells).
- Fast charge time :	within 1 hour.
- Abs.max. fast charge time :	1.5 hour time out.
- Charge currents :	625mA (1.25C) fast charge. 30mA (0.06C) trickle charge, (6 - 60mA setting range).
- Charge control methods :	-dV , timer , temperature optional.
- Switch mode frequency :	60kHz.
- Maximum continuous output power :	6.4W.
- Charger efficiency :	>75% at maximum output power.

3 BASIC CIRCUIT OUTLINE

3.1 Block diagram

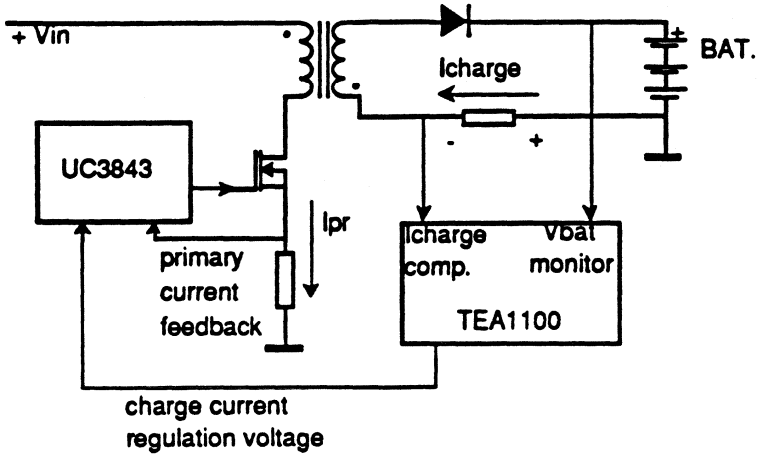

Fig. 1. Basic circuit diagram of the charger system example.

The essential parts are the supply flyback converter with its transformer, power switch and the IC UC3843 which drives the switch and controls the primary input current. The IC follows the primary current flow by sensing the voltage across a resistor in the primary loop.
At the secondary output side the battery is under the control of the TEA1100. This IC senses the battery voltage for save charge operation and it senses the output current via a current sense resistor in the secondary current loop. The current magnitude is referred by TEA1100 which provides an error feedback voltage for the stabilization of the charge current. This error voltage is fed back to the primary controller which translates the info into a correct duty cycle of the MOSFET drive pulses.

3.2 Current regulation loop

See figure 2.
The secondary output current is sensed at the sense resistor ,Rs-sec, and via voltage level shifting and RC smoothing, the residual voltage is compared to ground level by TEA1100. The dc error voltage is build up across the loop stability capacitor Cls. This voltage is, 4x amplified, available as output at the AO pin of the IC.
The small signal bandwidth of the AO signal has to be a distance below the switching frequency to ensure stability and therefore the error loop signal has a relative slow response time.

The overall response time can then be improved again by applying a feedforward, cycle by cycle, approach within the primary switching loop. Current mode controllers do respond to this as they drive the power switch under control of interacting error and primary current signals. The improved response time applies however only to rapid changes in the input voltage. A sudden change in the output condition is only corrected via the slower secondary to primary feedback.

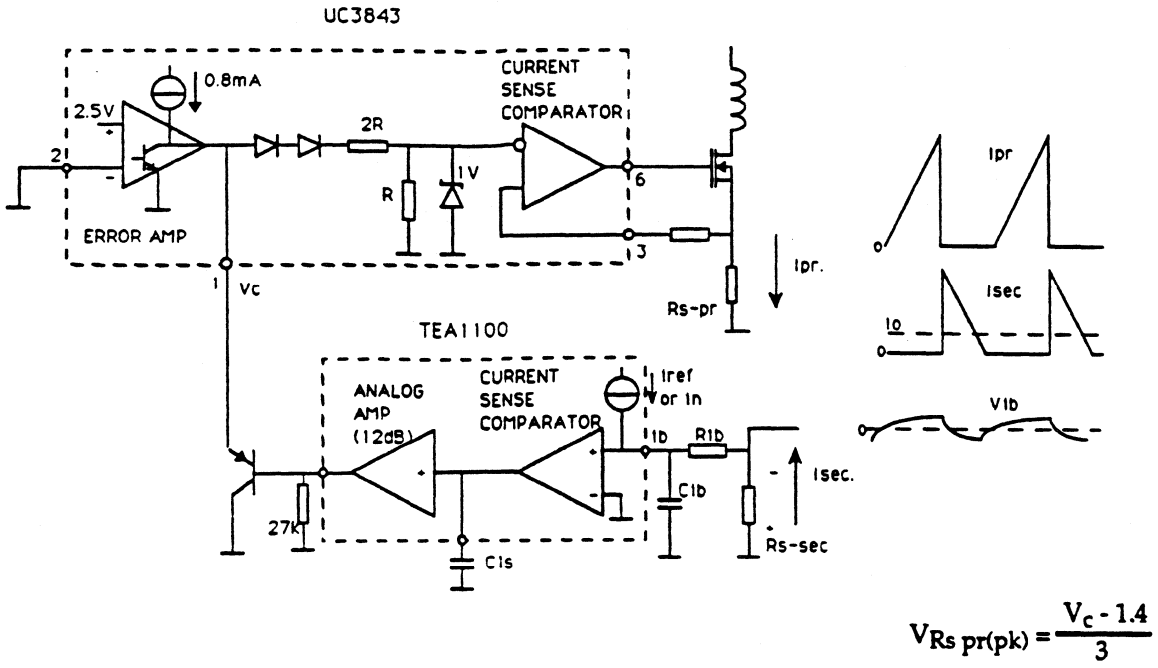

Fig. 2 The current regulation feedback loop diagram

The UC3843 is selected for primary control and power mosfet drive. The current comparitor which delivers the duty cycle controlled drive pulses, compares the primary peak current at Rs-pr with the error feedback voltage from TEA1100.
Peak current protection occurs when the peak voltage across the sense resistor reaches the UC3843 internal zener value, V_Z , which can range between 0.9 and 1.1V. Below the peak voltage value the duty cycle depends on the magnitude of error voltage at the Vc pin. The voltage error amp of UC3843 is set to function as a current source of typ 0.8mA with input pin 2 to common.
At the Vc pin, the voltage feedback active range is from 1.4V(diodes) to [3 x V_Z + 1.4V(diodes)]. The high level can so vary between 4.1 and 4.7V, (typ. 4.4V) depending on V_Z.
When TEA1100 is not initialized or is in the off period within the pulsating trickle charge mode, then its AO output floats. In this case or an other case of feedback absense the Vc pin is drawn to common via the PNP buffer which disables converter operation. On feedback signal from TEA1100 the converter is able to run.
In the non invert mode the AO amp sources current only and the maximum output voltage is 3.6V. Therefore the Vc voltage can reach a maximum of 3.6V plus the V_{BE} of the buffer: total 4 - 4.3V, which coincides with a comparitor sense level of 0.87 - 0.97V. Here an advantage appears of a tighter tolerance on the maximum Vc- or switch current peak level.

3.3 Current sensing parts

- Primary current sense resistor value: Rs-pr ≤ 0.87V/Ipr(pk)max. (Ipr(pk)abs max = 0.97V/Rs-pr).

- Secondary current sense resistor value : Rs-sec ≥ Iref x Rib / Io charge.

For sensing the correct output current, the triangle pulse sense voltage, analogue to the current shape, must be averaged and the residual ripple should be less than 160mV. Further smoothing of the error voltage

occurs in C_{LS}. (ref 1).

The required smoothing Rib x Cib network can be derived from the formula;

$$Rib \cdot Cib \geq \frac{1}{Vripple} \frac{(V_{pk} - V_{avg})^2}{2 \cdot V_{pk}} \cdot \delta sec \cdot T$$

were: $Vripple \leq 0.16V$

$V_{pk} = I_{sec\ pk} \times Rsense$
$V_{avg} = Isec_{avg} \times Rsense$
$\delta sec \cdot T$= Isec pulse time

The highest ripple voltage will be at maximum output power.

The ripple voltage on the LS capacitor is by approximation; $V_{Cls\ ripple} = \frac{V_{ib\ ripple} \cdot g_m}{8 \cdot f_{osc} \cdot C_{ls}}$

In section 5 the formulae above are used with the determined data.

4 POWER STAGE AND TRANSFORMER DESIGN

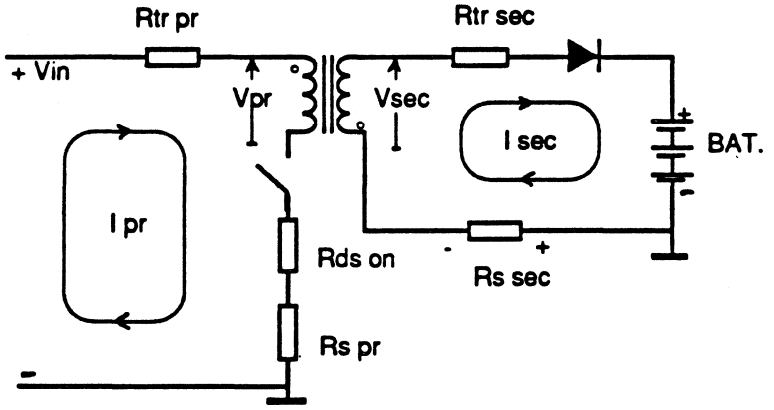

Fig. 3 The large signal power stage configuration

4.1 Transformer operation

The discontinuous current mode has been chosen because constraints on the feedback loop stability are minimal. Also the supply output power source characteristic is easier to handle than an output voltage source which is inherent to the continuous current mode operation.
At fixed frequency the limit case of discontinuous current operation, whereafter it changes to continuous current operation, is however different between a voltage regulated and a current regulated supply. With constant output voltage the limit case occurs at maximum power while with constant output current the limit occurs at minimum power, i.e. the lowest output voltage.
Figure 4 shows the current and voltage waveforms of the transformer at both maximum power and limit case with reduced power for the constant output current condition.

Transformer current and voltage waveforms at constant output current

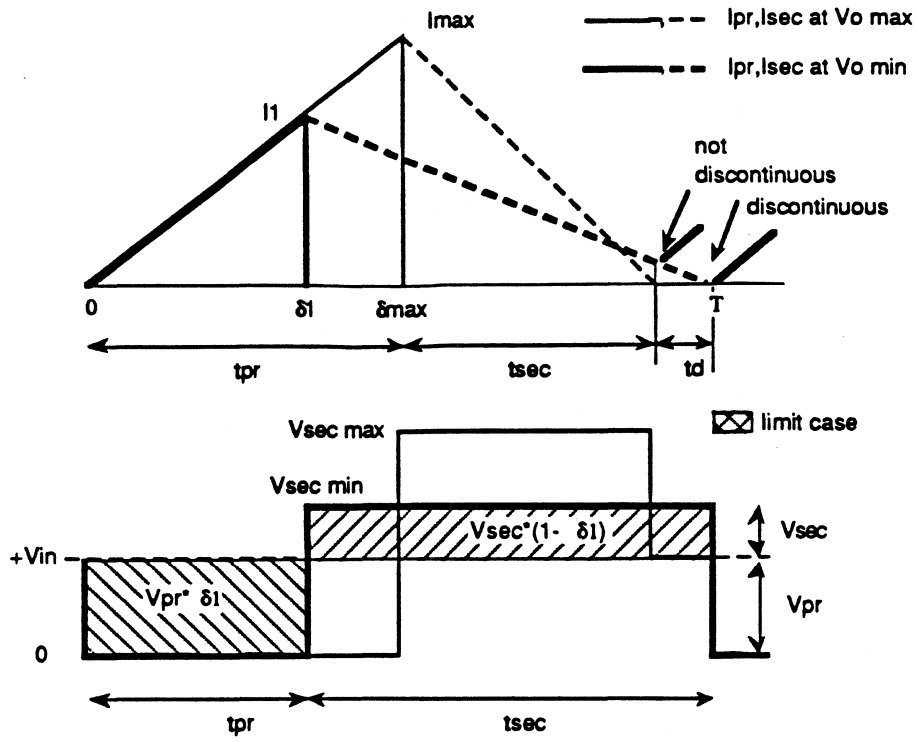

Fig. 4 Transformer current (a) and voltage (b) waveforms at constant current output

At maximum power the waveforms shows that the transformer is not fully utilised due to the introduced dead time in current. (Only a Self Oscillating Power Supply, SOPS, mode can prevent this dead time periode). Nevertheless, for a battery charger the transformer and supply performance with fixed frequency will hardly differ from the SOPS performance while interference-wise the fixed frequency is preferable.

4.2 Basic formulae for transformer operation.

Energy in transformer: $$E = \frac{1}{2} \cdot L \cdot I^2 \quad [1]$$

Peak current: $$I_{pk} = \frac{V_{pr}}{L_{pr}} \cdot t_{pr} \quad [2]$$

Primary on time: $$t_{pr} = \delta \cdot T \qquad (T = \frac{1}{f}) \quad [3]$$

Throughput power: $$P_{th} = E \cdot f \quad [4]$$

substitute 1,2,3,4: $$P_{th} = \frac{(V_{pr} \cdot \delta)^2}{2 \cdot L_{pr}} \cdot T \quad [5]$$

Limit discontinuous condition / constant output current;
(occurs at minimum V_{sec} and minimum V_{pr})

see shaded parts in fig. b $V_{pr(min)} \cdot \delta_1 = N \cdot V_{sec(min)} \cdot (1-\delta_1)$ were ($N = \frac{N_{pr}}{N_{sec}}$)

Duty cycle relation with secondary voltage; $\frac{\delta_1}{\delta_{max}} = \sqrt{\frac{V_{sec(min)}}{V_{sec(max)}}}$ [7]

Secondary fraction at maximum power: $\delta_{sec} = \delta_{max} \cdot \frac{V_{pr(min)}}{N \cdot V_{sec(max)}}$

or: $\delta_{sec} = \frac{V_{sec(min)}}{V_{sec(max)}} \left(\sqrt{\frac{V_{sec(max)}}{V_{sec(min)}}} - \delta_{max} \right)$ [8]

Dead fraction at maximum power: $\delta_d = 1 - \delta_{max} - \delta_{sec}$ [9]

Minimum duty cycle: $\delta min = \delta max \cdot \frac{Vpr(min)}{Vpr(max)} \cdot \sqrt{\frac{Vsec(min)}{Vsec(max)}}$ [10]

(at Vpr(max) and Vsec(min))

4.3 First shot at transformer size and loss

Let us assume that a feasable SMPS efficiency,η, is in the order of 70%. The maximum output power is 10.2V x 0.625A = 6.4W (Vo= 1.7V/cell x 6).
Core size can quickly be determined by the energy figure $L \cdot I^2$.

The required $L \cdot I^2 = 2 \times Po / \eta / f = 2 \times 6.4W / 0.7 / 60kHz = 3 \times 10^{-4}$ J.

- Size: Out of the RM cores*) data in fig.4 a selection is made for a RM6/i core with a standard range airgap of 0.15mm which maximum $L \cdot I^2$ value is 3.2×10^{-4}. [A_L = 250nH]

- Material: For 60kHz frequency a suitable core material is 3C85.

- Loss: The total dissipation in the transformer is the sum of the windings' copper and core losses. The thermal resistance of RM6 is about 75°C/W and when a temperature rise of 40°C can be accepted then the maximum dissipation is 0.53W.

  The core loss can be derived from the data in fig.5. which give watts per core volume with peak flux density B and frequency. This peak flux density refers to bidirectional flux swing. For the discontinuous operation the flux swing goes in one direction only and therefore the flux density is half the top flux which can be up to 320mT at 100°C. If B peak density is limited to 150mT then at 60kHz the core loss outcome is 120kW/m^3. The effective volume of RM6 is 1325mm^3 which gives a maximum core loss of 159mW.

  The copper loss is now restricted to 374mW which can equally be divided amongst the two windings.

*) In this SMPS example the RM core choice does not imply that it is the best overall choice. Other types should be considered as well. Acquaintance and possesion of RM types was the authors' selection reason.
For any customized supply, Philips magnetics department can offer the best and cheapest solution for your transformer requirement.

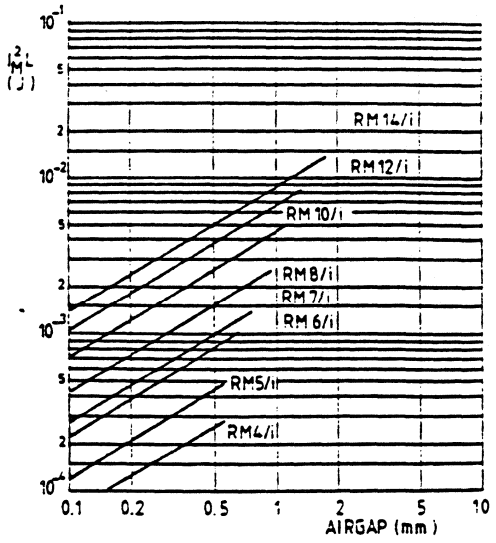

Fig. 5 Maximum energy versus airgap for RM range.

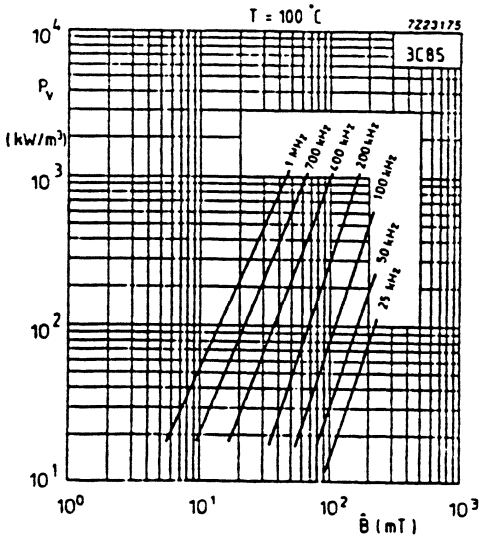

Fig. 6 Specific power loss versus peak flux density with frequency as parameter

4.4 Setting the design start parameters.

A completely empty cell can have a voltage that is near zero or even slightly negative but as soon as charging starts, a healthy cell will quickly restore its voltage to beyond 0.9V.
It is therefore unrealistic to include a very low output voltage condition into the transformer design limits as this might lead to a more bulky transformer due to less transformer utilization (increased dead time) at the high power operation.

- The design example is based on a transformer secondary voltage range factor of: $V_{sec(max)}/V_{sec(min)} = 2$
- A maximum duty cycle has to be asigned. Chosen is : $\delta_{max} = 0.5$
- Derived from [9] $\delta_{sec} \leq 0.45$. To allow for tolerances a wider margin is included into δ_d, so: $\delta_{sec} = 0.4$
- Secondary current sense resistor : $R_{s\,sec} = 0.2\Omega$

4.5 Calculations on the power stage

Contrary to that in a mains operated supply, the resistive losses in a low input voltage supply will have a higher influence on the transformation conditions. Therefore a more detailed calculation approach is followed which includes all power stage components. The calculation approach goes from secondary to primary side and applies to the limit case of maximum power conversion.
Series resistances with the transformer are taken not to affect the current ramp linearity in both primary and secondary currents.

Refer to the requirements data of the supply example (section 2) and the design start parameters (section above) to work out using a formula, the result which is given adjacent;

Maximum output power	$P_o = V_{o(max)} \cdot I_o$	6.4W
Average secondary pulse current	$I_{sec\ (pulse)} = \frac{I_o}{\delta_{sec}}$	1.56A
Peak secondary pulse current	$I_{sec\ (pk)} = 2 \cdot I_{sec\ (pulse)}$ [triangle waveform]	3.13A
RMS value of output current	$I_{RMS} = I_{sec\ (pk)} \sqrt{\frac{\delta_{sec}}{3}}$	1.14A
Square of RMS output current	$I_{RMS}^2 = \frac{4 \cdot I_o^2}{3 \cdot \delta_{sec}}$	1.3A
Loss secondary sense resistor	$P_{R\ sense} = I_{RMS}^2 \cdot R_{sense}$	0.26W
Loss secondary winding [section 4.3]	$P_{tr\ Rsec} = \frac{P_{copper\ max}}{2}$	0.19W
Max. resistance secondary winding	$R_{tr\ sec} = \frac{P_{tr\ Rsec}}{I_{RMS}^2}$	0.15Ω
Secondary diode loss	$P_{D\ sec} = I_o \cdot V_{D(max)}$ [$V_{D(max)}$= 1V]	0.63W
Transformer secondary power	$P_{tr\ sec} = P_o + P_{tr\ Rsec} + P_{R\ sec} + P_{D\ sec}$	7.45W
Transformer secondary voltage	$V_{tr\ sec} = V_o + V_{D(max)} + \{I_{sec\ (pulse)} \cdot (R_{s\ sec} + R_{tr\ sec})\}$	11.75W
Transformer primary power (Leakage inductance loss is neglected)	$P_{tr\ pr} = P_{tr\ sec} + P_C$	7.61W
Transformer primary power also	$P_{tr\ pr} = V_{in(min)} \cdot I_{in} - P_{Rpr(tot)}$	

The primary current has to be deducted and known are; $V_{in(min)}$, primary winding loss and the peak voltage across the primary sense resistor. $R_{DSon(max)}$ of the MOSFET is also required.
For the resistive losses the RMS current is essential.

For a MOSFET selection the approximate primary input current is:

$$I_{in} = Po / Vin\ (min) / \eta = 6.4 / 9 / 0.7 = 1A$$

$$I_{pr\ RMS}^2 = 4 x I_{in}^2 / 3 / \delta_{max} = 2.6\ A^2$$

If MOSFET dissipation ≤ 0.05x Pin = 0.45W then its on resistance ≤ 0.45/2.6 = 0.18Ω at Tj = 100°C.

At Tj = 25°C R_{DSon} ≤ 0.18/1.4 = 0.13Ω.

Within the 60V range, BUK442 ,452 or 472 can be applied.

To continue, first some formulae to enable further calculations.
Energy is built up during the on time period, δ_{max}, so;

Transformer primary power	$P_{tr\ pr} = I_{pr(pulse)} \cdot V_{tr\ pr(pulse)} \cdot \delta_{max}$	[11]

where $V_{tr\ pr(pulse)} = V_{in} - V_{Rpr\ tot(pulse)}$ [12]

RMS value of primary current $I_{prRMS} = 2 \cdot I_{pr(pulse)} \cdot \sqrt{\frac{\delta_{max}}{3}}$ (triangle waveform [13]

Maximum primary winding resistance $R_{trpr} \leq \frac{3 \cdot P_{Rtr\ pr}}{4 \cdot I_{pr(pulse)}^2 \cdot \delta_{max}}$ [14]

Average primary winding pulse voltage $V_{Rtr\ pr(pulse)} = \frac{3 \cdot P_{Rtr\ pr}}{4 \cdot I_{pr(pulse)} \cdot \delta_{max}}$ [15]

Average primary sense pulse voltage $V_{Rs\ pr(pulse)} = \frac{V_{Rs\ pr(pk)}}{2} = 0.45V$ [section] [16]

Substituting [11 - 16];

Average primary pulse current $I_{pr\ (pulse)} = \frac{P_{trpr}/d_{max}}{(V_{in}-0.45) - I_{pr(pulse)} \cdot R_{DSon} - \frac{3 \cdot P_{Rtrpr}}{4 \cdot I_{pr(pulse)} \cdot \delta_{max}}}$ [17]

solve $I_{pr\ (pulse)}$ by $I_{pr\ (pulse)} = \frac{-b \pm \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a}$ were: $a = R_{DSon(max)}$, $b = -V_{in} + 0.45$, $c = \frac{\frac{3}{4} P_{Rtrpr} + P_{trpr}}{d_{max}}$ 1.89A

Primary peak current $I_{pr\ (pk)} = 2 \cdot I_{pr\ (pulse)}$ (triangular waveform) 3.78A

RMS value of input current $I_{prRMS} = I_{pr\ (pk)} \sqrt{\frac{\delta_{max}}{3}}$ 1.54A

Primary sense resistor $R_{s\ pr} \leq \frac{0.9}{I_{pr(pk)}}$ 0.24A

Primary winding resistance $R_{tr\ pr} \leq$ [14] 79mΩ

Primary resistive loss $P_{Rtot\ pr} = I_{prRMS}^2 \cdot (R_{s\ pr} + R_{DSon} + R_{tr\ pr})$ 1.18W

Input power $P_{in} = P_{tr\ pr} + P_{R\ pr}$ 8.79W

Transformer primary voltage $V_{tr\ pr} = V_{in\ (min)} - \{I_{pr\ (pulse)} \cdot R_{pr(tot)}\}$ 8.06V

Transformer winding ratio $N = \frac{N_{pr}}{N_{sec}} \geq \frac{d_{max} \cdot V_{trpr}}{d_{sec} \cdot V_{trsec}}$ ≥0.86

Primary inductance $L_p \leq \frac{V_{trpr} \cdot \delta_{max}}{I_{pr(pk)} \cdot f}$ 17.8µH

Transformer windings $N_{pr} \leq \sqrt{\frac{L_p}{A_L}}$; $N_{sec} \leq \frac{N_{pr}}{N}$ resp. < 8.44 ; < 9.8

The transformer windings must consist of whole turns numbers: Npr; Nsec = 8 ; 9
The practical primary inductance with 8 turns: N_{pr} = 16µH,

The lower N_{pr} changes the primary peak current to maximum: $I_{pr\,pk} = 3.78\sqrt{\frac{17.8}{16}}$ = 4A

and the primary sense resistor becomes: $R_{s\,pr} \leq 0.9/4$ = 0.22Ω

Primary blocking voltage across the switch: $V_{pr}\,max = V_{in\,(max)} + V_{tr\,sec} \cdot N + \Delta V$ = 30.5V + ΔV

$(\Delta V = I_{pr\,(pk)}\sqrt{\frac{L_L}{C_{tr}}})$; for ΔV=20V, L_L/C_{tr} < 27.7 nH/nF

The transformer windings were bifilar wound which gave a very low leakage inductance. The ΔV was 20V at maximum power and a snubber could be omitted. In the case a snubber is required then a zener diode, V_Z = ΔV max, in series with a reverse blocking diode can be applied across the primary winding.

5 TEA1100 SETTINGS

In this system the current feedback signal is derived from the analog output of TEA1100, so there is no link between the SMPS frequency and the TEA1100 frequency like in the system as in ref.1. (chpt.8)

Here following the TEA1100 calculation procedure with the formulae is given . It is also possible to get results quickly from the nomograph given in fig. 8.

5.1 Time settings

Start with the requirement for the maximum fast charge time, TO, which should be about 25 - 50% above the maximum expected 1Hr charge time by -ΔV cut-off. A 50% longer TO = 1.5Hr. (This can be altered by changing the oscillator capacitor value).

Directly related to TO are:

- Monitor disable time at start of charge $t_{disable} = 2^{-5} \times TO$ = 2.8 min.
- Trickle charge repetition time $T_{trickle} = 2^{-14} \times TO$ = 330 ms.

Now a frequency has to be chosen using the pre scaler factor p = 1, 2 or 4.
Choosing p=1 by setting (PR [pin8] to Vsource [pin6]);

- Oscillator frequency $f_{osc} = \frac{2^{26} \times p}{TO}$ = 12.4kHz
- Selection of Rref and Cosc by $R \times C = \frac{1}{0.93 \times f_{osc}}$ = $87 \cdot 10^{-6}$
- 12.5k < Rref < 125k — Rref selected = 27kΩ; Cosc = 3.3 nF

From fosc or Tosc derive;

- Monitor sampling repetition $T_{sampling} = 2^{16} \times T_{osc}$ = 5.3s
- Monitor sampling charge inhibit period $t_{inhibit} = 10 \times T_{osc}$ = 805µs
- Trickle charge ON duration $t_{trickle} = 0.75 \times 2^{9} \times T_{osc}$ = 31ms

- Duty cycle trickle charge pulses $\delta\,\text{trickle} = \frac{t\,\text{trickle}}{T\text{trickle}} = 9.4\%$

5.2 Charge current settings

- Current reference resistor;

$$\text{Rib} = \frac{\text{Ich fast} \times \text{Rref} \times \text{Rsec sense}}{1.25} = \frac{625\text{mA} \times 27\text{k} \times 0.2\Omega}{1.25} = 2.7\text{k}\Omega$$

- Trickle charge current;

Rn not applied Ich trickle $= \frac{\text{Ich fast}}{2} \times \delta\,\text{trickle} = 30\text{mA}$

Rn applied (≥Rref) Ich trickle $= \text{Ich fast} \times \frac{\text{Rref}}{\text{Rn}} \times \delta\,\text{trickle} =$

$25\text{k} < \text{Rref} < \text{Rn} < 250\text{k}$

Rn = Rref ; 60mA

Rn = 250k ; 7mA

5.3 Current sense input filter

The Cib, Rib time constant should be as small as possible to ensure quick stabilization of the charge current following an interrupt. This occurs at start up, monitor sampling and trickle charge. Therefore allow for the maximum ripple of 0.16V at the IC sense input, ib.
With the formula in section 3.3 the RC can be determined by filling in the derived data (section 4.4, 4.5)

$$\text{Rib}\cdot\text{Cib} \geq \frac{1}{0.16} \frac{(0.626 - 0.125)^2 \cdot 0.4}{2 \cdot 0.626 \cdot 60 \cdot 10^3} \geq 8.4 \cdot 10^{-6}$$

Rib = 2k7 so Cib is minimal 3.1nF and a practical value is 3.3nF.

5.4 Vac Setting

The battery voltage has to be adapted to within the Vac monitor input voltage range via a divider.
In appendix 1 divider resistor values with applied number of battery cells are listed for quick resistor selection.
In this design a divider ratio p = 0.33 is chosen (56kΩ and 27kΩ) which allows recording up to a maximum battery voltage of 11.84V (~2V/cell). At an open output, charge supply protection activates at and beyond 13V.
The -ΔV cut-off sensitivity of 1% can be made more sensitive if required in case of NiMH battery use. A value adjustment of the 56KΩ resistor which is connected in series with a low voltage avalanche diode out of the Philips PLVA400A range is all that is needed to achieve a -ΔV of about 0.5%. (Details in ref.1 or 2)

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5.5 Temperature sensing

An extra protection against fast charge operation when the battery temperature is out of a safe range can be added. A NTC thermistor characteristic is adapted to the sense input of TEA1100 by one or two resistors and a bias voltage. Details are given in Appendix 2.

6 FEEDBACK LOOP STABILITY

In figure 2, chapter 4, the various stages within the current regulation feedback loop have been given. For stability, loop compensation can be set with a capacitor at the C_{ls} node of TEA1100.

The transfer characteristics of the stages are;

6.1 SMPS stage

Based upon formula [ ] the output current can be expressed as: $$I_o = \frac{L I_{pr}^2}{2 V_o} f \eta \quad [21]$$

The primary peak current is also : $$I_{pr} = \frac{(V_c - 1.4)}{3 R_{s\,pr}} \quad [22]$$

Substitude 21,22: $$I_o = \frac{(V_c - 1.4)^2}{V_o} \cdot \frac{L \cdot \eta \cdot f}{18 \cdot R_{s\,pr}^2}$$ where the latter term is constant; [23]

k = 0.88 at this example.

For low frequencies the small signal admittance is determined by the differential $\frac{\partial I_o}{\partial V_c}$ at the adjustments of I_o and V_o ;

SMPS transfer: $$Y_3 = \frac{\partial I_o}{\partial V_c} = \frac{2 \cdot (V_c - 1.4)}{V_o} \cdot k \text{ or } 2 \cdot \sqrt{\frac{I_o \cdot k}{V_o}}$$ by substitution V_c as in [23]. [24]

The SMPS stage ac voltage gain $$H1 = \frac{\partial V_{Rs\,sec}}{\partial V_c} = 2 \cdot Rs\,sec \sqrt{\frac{I_o \cdot k}{V_o}} \quad [25]$$

The highest voltage gain will occur at maximum I_o and minimum V_o.

RESULTS FOR H1 : at V_o = 2 V H1 = 0.21x or -13.6dB
at V_o = 10.2V H1 = 0.1x or - 20 dB

The voltage gain is independent of the frequency but a phase shift lag , proportional to frequency, will occur because of the converter flyback operation. By measurement the phase shift was determined to be ;

$\varphi_1 \approx -2^o/kHz$

6.2 TEA1100 regulation stage.

The voltage transfer of the input filter $$H2 = \frac{Vib}{V_{Rs\,sec}} = \frac{1}{\sqrt{1+(\omega Rib\,Cib)^2}} \quad [26]$$

$\varphi_2 = -\arctan(\omega\, Rib\, Cib)$.

- The voltage transfer of the transconductance error amp stage with a capacitor Cls at output (g_m = 250µA/V ; Ro = 4.5MΩ)

$$H3 = \frac{Vls}{Vib} = g_m \frac{Ro}{\sqrt{1+(\omega\, Ro\, Cls)^2}} \quad [27]$$

$\varphi_3 = -\arctan(\omega\, Ro\, Cls)$

The voltage transfer of the AO amp $H4 = \frac{Vao}{Vls} = 4x \text{ or } 12dB \quad (Vao = Vc)$ [28]

The unity bandwidth of AO is 4MHz so $\varphi_4 = 0°$ at frequency < 100kHz

6.3 Total loop response

The loop gain has to be well below zero at the SMPS switching frequency of 60kHz. The unity gain can be chosen at a frequency less than one third the switching frequency, so ≤ 20kHz if the phase margin is adequate ≈ 50 degrees.

The total gain is H1 x H2 x H3 x H4 where H1 x H4 = -2dB max. This gain is frequency independent within the relevant frequency range. At unity loop gain; H2 x H3 = 2dB.
The frequency at unity gain depends on φ_1 and φ_2 . For φ_3 -90° can be filled in when only a compensation capacitor C_{ls} is applied: single low frequency pole, no zero.

The sum of φ_1 and φ_2 is $\frac{-2 \cdot 10^{-3}}{f_u}$ - arctan $2 \pi f_u$ Rib Cib and is allowed to be -180 + 90 + 50(margin) = -40°.

$$f_u \leq 9kHz$$

At 9kHz ; H2 = - 1.8dB and φ_2 = -27°. The residual gain for H3 = 3.8dB.

Formula [27] can be rearranged to get the required Cls = $\frac{1}{\omega_u \cdot H3 \cdot Ro} \sqrt{(g_m \cdot Ro)^2 - H3^2}$. For H3 < 200x this formula can be simplified to: $Cls \approx \frac{g_m}{\omega_u \cdot H3}$. The required Cls is 3nF minimal, 3.3nF as practical value.

Figure 7 gives the bode plot of the closed loop response.

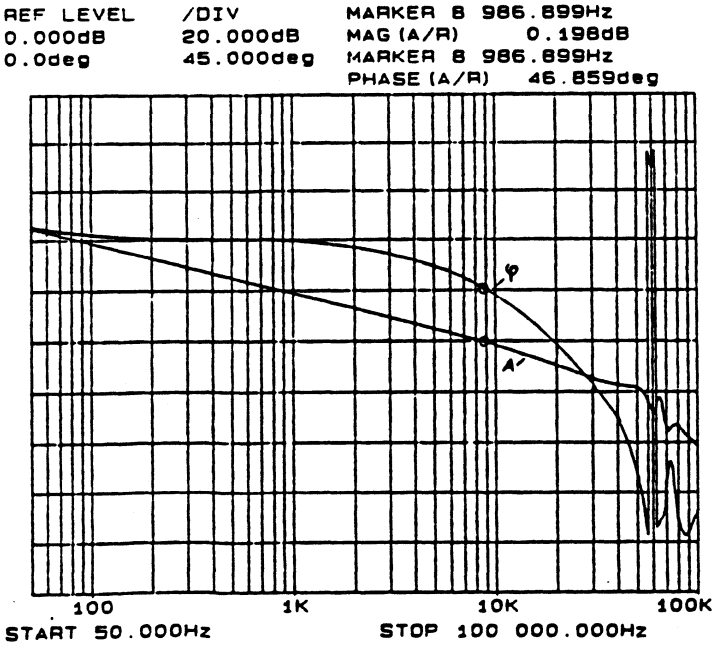

Fig. 7 Closed loop bode plot

7 DESIGN RECOMMENDATIONS

Where high rated pulse currents flow , as in the primary and secondary power loops, care has to be taken for the proper component selection and a well thought out PCB layout
Especially for the low ohmic current sense resistors, avoid a wire-wound type even when specified as low inductive because large voltage spikes is what you get at current switching. Use carbon or metal film types and use mutiple units in parallel to obtain a low value or power rating.

Buffer and decoupling capacitors have to cope with steep pulse currents and should have a low ESR value.

Make the PCB current power loops as close as physically possible. Prevent sharing of ground tracks between the power and small signal circuitries by using star configurations.

Place the supply voltage decoupling capacitor of TEA1100 close to the IC supply and ground pins. A great part of this IC consists of digital circuitry and possible interference from the input supply (insufficient filtering especially with a simple mains adapter) should be filtered via the capacitor.

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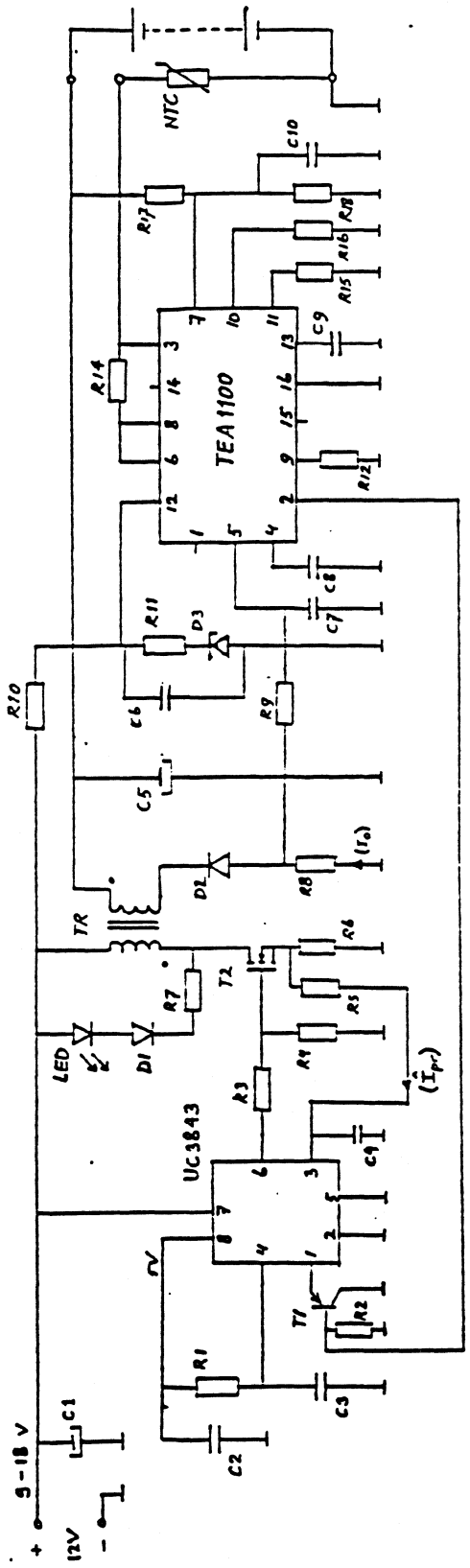
2 TEA1100(T) Preliminary specification. April 1992.
3 DATA HANDBOOK , linear products IC11; sections: AN125, AN1261, UC3843.
4 3C85 HANDBOOK First in Ferrites. 12NC: 9398 345 90011.
5 DATA HANDBOOK, Soft Ferrites,MA01 12NC: 9398 174 50011.
6 SPO/AN91007 Mains Powered Fast NiCd Battery Charger using TEA1100.
7 SPO/AN92004 TEA1100 battery Charger with Linear Regulator.

9 CIRCUIT DIAGRAM



6 NiCd CELLS (550mAhr) IC CHARGER, Vin=12V.

Fig. 7 Charger diagram

10 PARTS LIST

Resistors	Value	Series		Part no.
R1	10k	MRS16T	1%	2322 157 31003
R2,4,15,18	27k	SFR16T	5%	2322 180 53273
R3	27Ω	SFR16T	5%	2322 180 53279
R5	1K	SFR16T	5%	2322 180 53102
R6	0.22Ω			
	= 5x1.1Ω in parallel	MRS25	1%	2322 156 21108
R7	620Ω	SFR16T	5%	2322 180 53621
R8	0.2Ω			
	= 5x1Ω in parallel	MRS25	1%	2322 156 21008
R9	2.7k	MRS16T	1%	2322 157 32702
R10	300Ω	SFR16T	5%	2322 180 53301
R11	240Ω	SFR16T	5%	2322 180 53241
R14	t.b.f.	SFR16T	5%	2322 180 5
R16	27k	MRS16T	1%	2322 157 32703
R17	56k	SFR16T	5%	2322 180 53563

Capacitors				
C1, C5	220µF	RLI 135		2222 135 66221
C2	10nF	ceremic		2222 629 09103
C3	2.7nF	KP	1%	2222 424 42702
C4	470pF	ceramic		2222 630 08471
C6	100nF	MKT	10%	2222 370 11104
C7,8	3.3nF	ceramic		2222.630 09332
C9	3.3nF	KP	1%	2222.424 43302
C10	680pF	ceramic		2222 630 08681

Semiconductors		
T1	BC557B	9332 026 20126
T2	BUK443-60B	9332 546 60127
D1	BAV18	9331 892 00153
D2	BYD74B	9337 537 40153
D3	BZX79 C7V5	9331 177 60153
D4	LED	9338 501 20112
IC1	UC3843	
IC2	TEA1100	

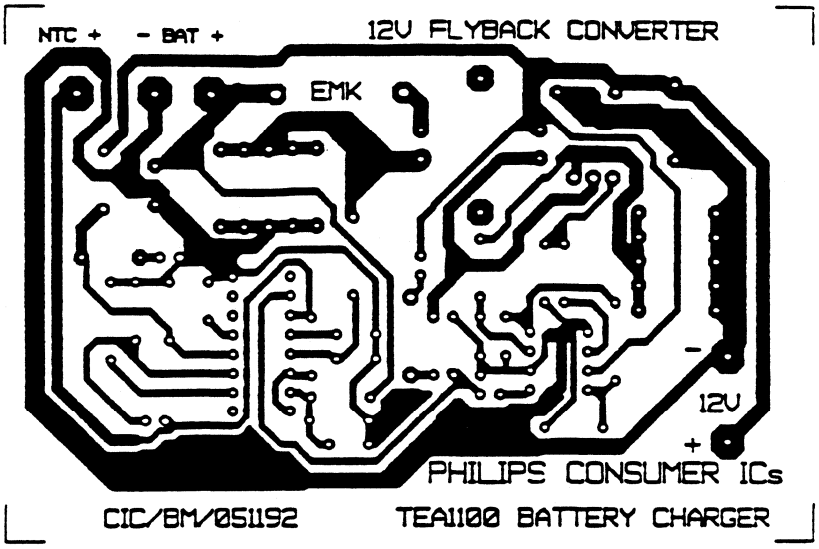
Transformer

RM6/i core set , gap= 0.15mm , 3C85 material ,(Al=250)	4322 025 05069
Coil former	4322 021 34511
Clips 2x	4322 021 34301

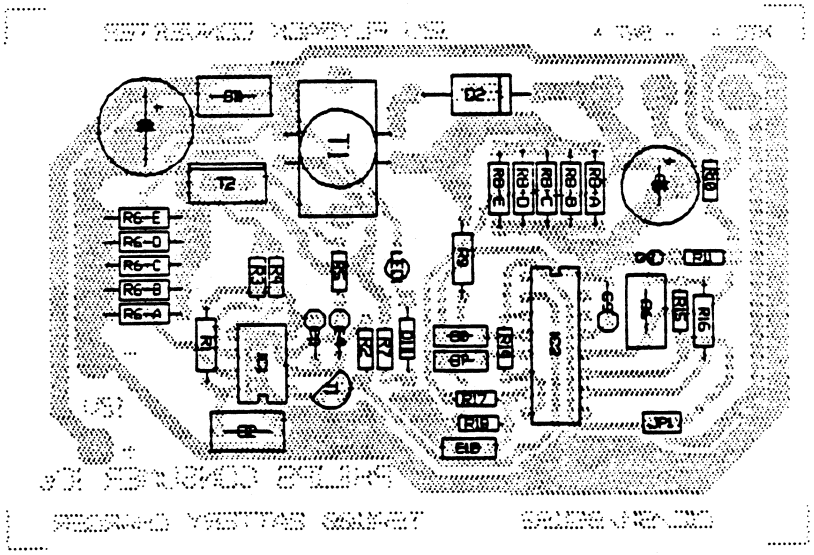
Lp=16µH , primary winding: 8 turns, 0.35mm wire
secondary winding: 9 turns, 0.35mm wire

11 PCB LAYOUT

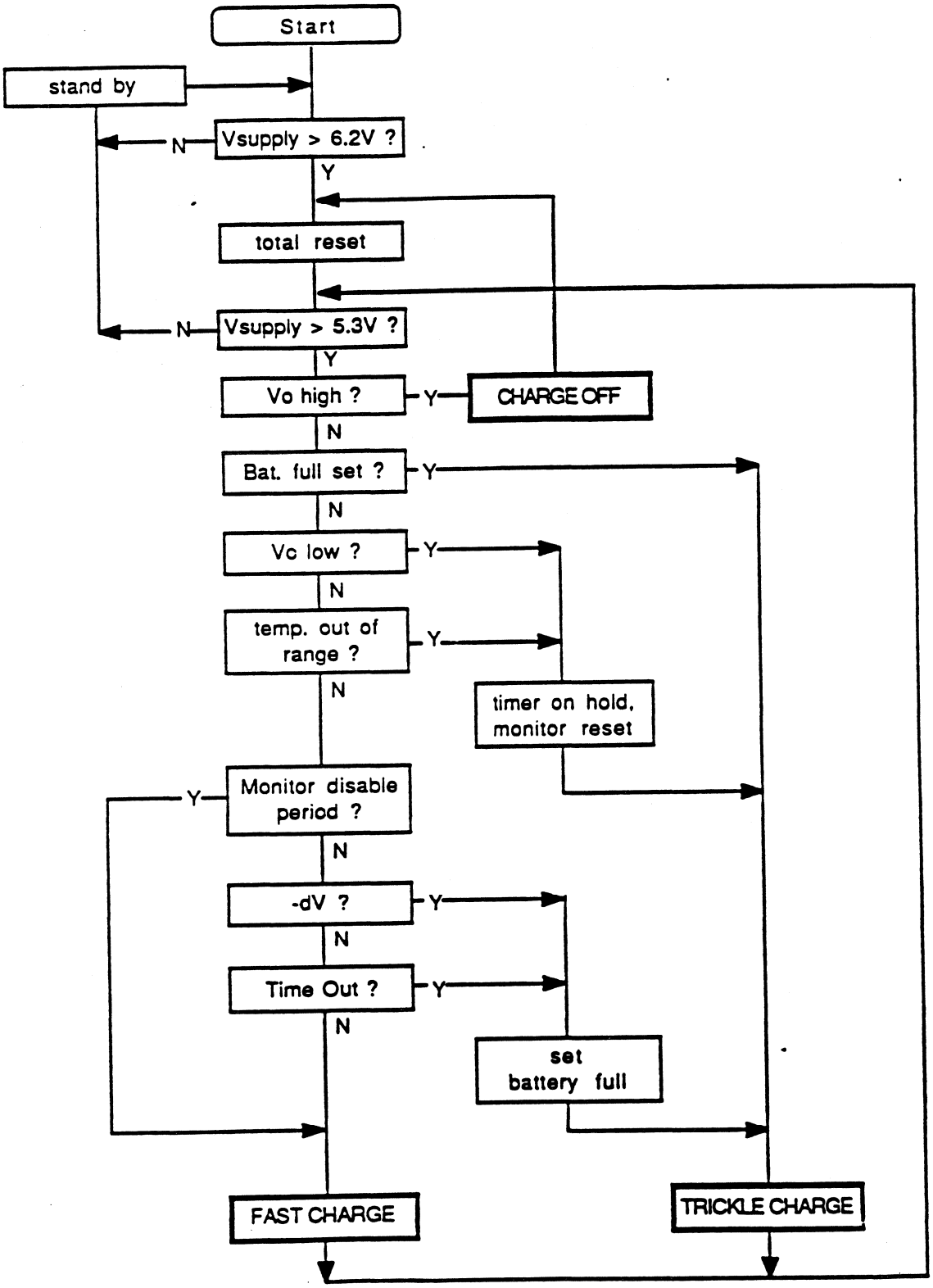
Copper side



Components side



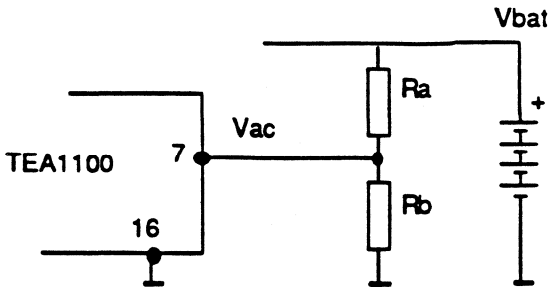
Appendix 1



TEA1100 charger flow diagram

Appendix 2

Resistor divider selection for TEA1100 sense input adaptation to the battery.



$$\frac{Ra}{Rb} \geq \frac{V_{BATmax}}{3.85} - 1$$

V_{BAT} high protection $\geq 4.25\ (1+\frac{Ra}{Rb})$

Cell number	2	3	4	5	6	7	8	9	
V_{BAT} max (1.7V/cell)	3,4	5,1	6,8	8,5	10,2	11,9	13,6	15,3	V
Ra ≥	12	12	22	39	47	68	82	91	kΩ
Rb	-	27	27	27	27	27	27	27	kΩ
V_{BAT} high protection ≥	4,3	6,1	7,7	10,4	11,6	15	17,2	18,6	V

For the design has been chosen : Ra = 56kΩ ; Rb= 27kΩ
where;

V_{BAT} sense max. = 11.84V (2V/cell)
V_{BAT} protection ≥ 13V

The division ratio is the key factor and the absolute resistor values can be chosen within a broad range.
The lower impedance is limited by discharge consideration while the higher impedance should remain low compared to the input impedance of the Vac pin 7 which is more than 200MΩ.
The lower impedance can be seen in relation with the batteries' self discharge. When assumed that the maximum capacity of a unloaded battery reduces by 30% over the first month (720 hours), then the average equivalent self discharge current in 500mAhr battery is in the order of ;

$$\frac{\text{capacity x loss}}{\text{period}} = \frac{500\text{mAhr x } 0.3}{720\text{hr}} = 0.21\text{mA}.$$

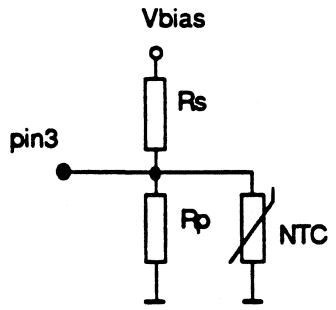
The imaginary battery discharge resistor is about; $\frac{1.27\text{V x cell number}}{\text{Idischarge}} = \frac{1.27 \times 6}{0.21} = 36\text{k}\Omega.$

The total divider load resistance in the table above is based on twice the imaginary discharge resistor in a battery of 500mAhr. For higher capacity ratings the given divider resistors can also be used.

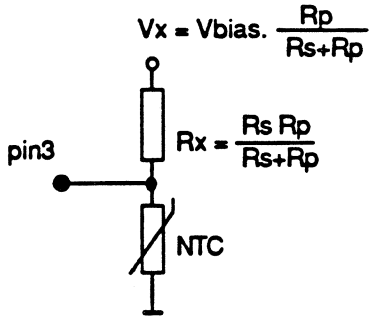
For applications with maximum 2 cells battery no Vac divider is required but a series resistor with the Vac input must be present to limit clamp current at 4.25V , protection level, in case the battery is removed while the charger is on. The limit Vac clamp current is ± 1mA.

Appendix 3

Battery NTC thermistor adaptation to TEA1100 temperature sense input.



Temperature sense network



Equivalent circuit

For the low and high temperature levels the corresponding R_h and R_l thermistor resistance values need to be derived

The following calculations lead to the required battery serie-, parallel resistor and the bias voltage;

low temperature limit , NTC resistance :	R_h	
high temperature limit, NTC resistance :	R_l	ratio; $p = \frac{R_h}{R_l}$
TEA1100 upper threshold	Vh = 3V	
lower threshold	Vl = 0.81V	range; $\Delta V_t = 2.19V$

If $k = \frac{\Delta V_t}{(p \cdot V_l) - V_h}$ then $Rx = k \cdot R_h$; $Vx = V_h (1+k)$

V_B = constant bias voltage ;

$(V_B \geq Vx)$

$$Rs(eries) = \frac{k}{3(1+k)} \cdot V_B \cdot R_h$$

$$Rp(arallel) = \frac{k}{V_B - 3(1+k)} \cdot V_B \cdot R_h$$

When the B value of the NTC is used then ;

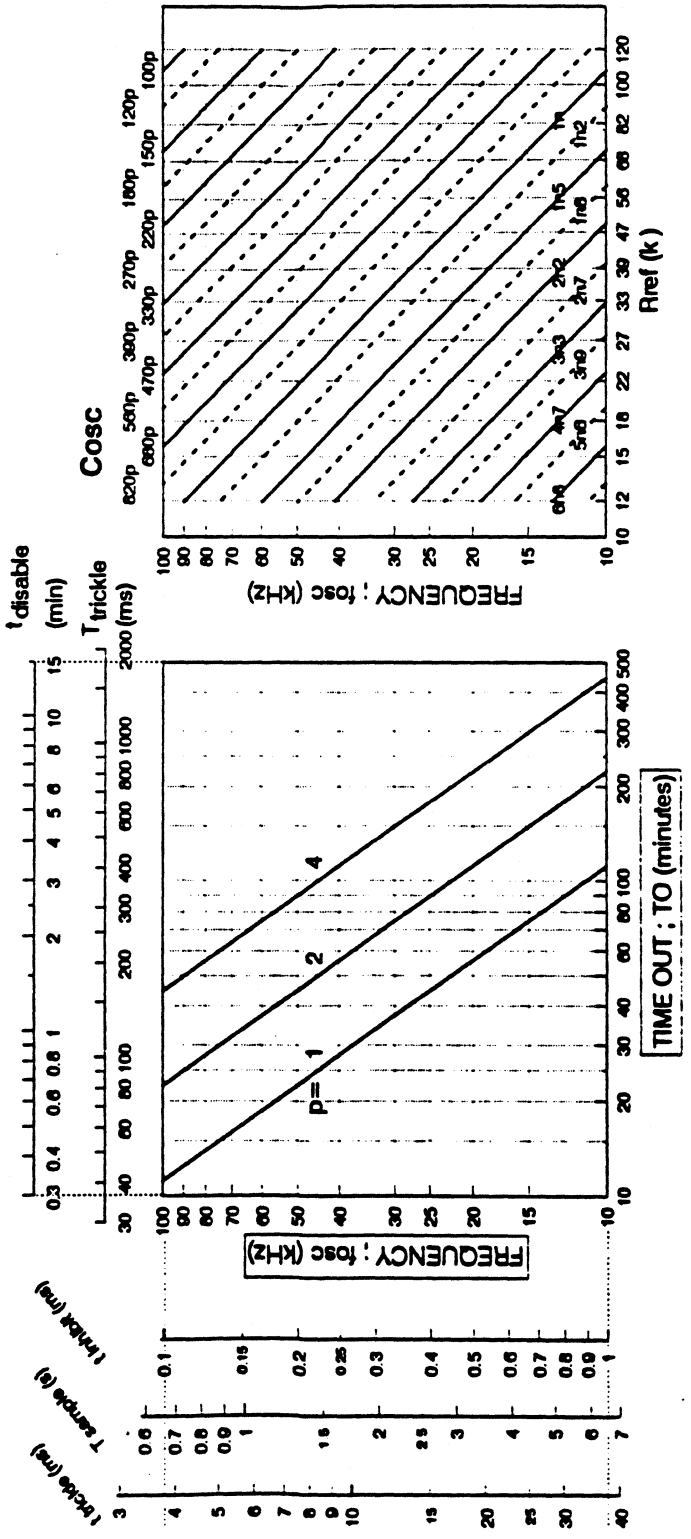
$$p = e^{B \cdot \left(\frac{1}{Tl} - \frac{1}{Th}\right)}$$ T is in Kelvin.

$$R_h = R_{25} \cdot e^{B \cdot \left(\frac{1}{Tl} - \frac{1}{298}\right)}$$

Note: Without temperature sensing ; a) i.s.o. NTC use resistor with same value of Rx (=R14) or
b) if resistor terminates pin11 then connect pin 3 to pin11 and skip Rx.

Appendix 4

TEA1100 timing and related components charts



NOMOGRAM OF TIME SETTINGS IN TEA1100

Application Note

ICs for BATTERY MANAGEMENT

TEA1100 Battery Charger with Linear Regulator

Report No: SPO/AN92004 a

R Verney

Product Concept & Application Laboratory Southampton, England.

Keywords
TEA1100
Fast Battery Charger
NiCd
NiMH
Linear Regulator
Cordless Telephone

Date : 08 OCT 1992
Pages : 18

Summary:

The fast NiCd and NiMH battery charger described in this report uses a TEA1100 control circuit, with a simple linear current regulator to provide precise battery charging. It is suitable for small to medium sized battery packs with charge times between 30 minutes and 5 hours. Typical applications include Cordless Telephone, Personal Audio and small domestic appliances.

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1. INTRODUCTION

The TEA1100 fast charge monitor and control circuit features -dV and timer charge cutoffs, with over and under temperature protection of the batteries. The control circuit is a versatile feature which is suited to all applications; PWM (switch mode), linear regulated supply, or simple non-regulated supply.

Where charge currents are low, or where the electrical noise of a SMPS circuit is unacceptable, a linear regulator circuit provides the best solution to current control with TEA1100.

Key Features:

- TEA1100 provides all battery management functions.
- Fast battery charging.
- Long battery life.
- Simple circuitry - easy to design.
- Low cost.

2. CIRCUIT DESIGN

The linear regulator is formed using the analogue control signal available from the AO pin (pin 2) of the TEA1100, a drive transistor, and a series pass transistor.

A circuit diagram is shown in Fig 1.

2.1 Linear Regulating Pass Transistor and Driver

T1, T2:

T1 and T2 are chosen appropriate to the voltage and power levels present. A heatsink must usually be fitted to T1. At the higher power levels, a large heatsink will be required. A switch mode solution should be carefully considered when power output exceeds 5 W.

D1:

Diode D1 prevents forward bias of the collector base junction of T1 occurring when batteries are inserted but no power applied. This prevents battery discharge.

R2:

R2 is chosen to provide sufficient base drive current to T1.

Table 1 Component Choice

Max no of cells	Max charge current	T1	T2	D1	R2
10	350 mA	BD132	BC549	IN4001	180R
10	1 A	BDT60A	BC635	IN4001	180R
10	1.2 A	BDT60A	BC635	IN5401	180R
6	2.2 A	BDT60A	BC635	IN5401	180R
3	3 A	BDT60A	BC635	IN5401	100R

2.2 Setting the System Timings

The system timings can be freely chosen to set the maximum time spent in fast charge, termed 'Time Out' period.

C3:

C3 sets the clock frequency, and hence all system timings.

Tosc	=	$0.93 \times R6 \times C3$
Time Out	=	$Tosc \times 2^{26} \times p$
Sample repetition	=	$Tosc \times 2^{16}$
Trickle repetition	=	$Tosc \times 2^{12} \times p$

where p is the prescaler factor set by the PR pin.

p = 1 PR = Vsource (pin 6), p = 2 PR = open, p = 4 PR = GND.

The prescaler setting affects the ratio of fast charge to trickle charge currents. With p = 1, the range of ratios is 10:1 to 20:1, p = 2, 20:1 to 40:1, p = 4, 40:1 to 80:1.

2.3 Setting the Charge Currents

R1, R3, R6, R7:

R1, the current sensing resistor should be chosen to give a voltage between 50 and 200 mV. This ensures accuracy, while keeping power loss in the resistor to a minimum.

R6, R7 determine the fast and trickle charge reference currents respectively. In turn, these reference currents, in combination with R1 and R3, set the charge currents.

For R6 a value of 27 k can usually be used, R3 and R7 can then be chosen appropriately.

I fast = Reference current (fast) × resistor ratio.

$$I\,fast = \frac{1.25 \times R3}{R6 \times R1}$$

Therefore, having set R6 and R1:

$$R3 = \frac{R6 \times R1 \times I\,fast}{1.25}$$

Values for R3 will usually be between 1 k and 10 k.

$$I\,trickle = \frac{1.25 \times R3 \times 0.094}{R7 \times R1 \times p}$$

Therefore:

$$R7 = \frac{1.25 \times R3 \times 0.094}{I\,trickle \times R1 \times p}$$

where p is 1, 2, 4 set by PR pin. See Section 2.2.

NB: 1 If R7 is greater than twice R6, it can be omitted, and a default reference current in trickle charge will be taken of half that used in fast charge.

2 R7 should generally not be less than R6, because the pulse of trickle current should not be of greater instantaneous magnitude than the fast charge current. In certain circumstances, such as where a supply of large enough current capability is available, this may be permissible however.

2.4 Control Loop Components

R2, R10:

To prevent excessive loop gain, local negative feedback is applied to T2 by R2. A value is chosen to ensure sufficient base current for T1 with AO at its maximum of 3.6 V, and allowing for minimum gain in T1. R10 ensures correct turnoff of T1.

C2:

C2 is connected to maintain loop stability. For the linear regulator its value is noncritical and can be found empirically. The linear

regulator is inherently very stable with rapid transient response. A value of 10 nF will usually suffice.

NB: The capacitor on the IB pin (pin 5), fitted in SMPS circuits, must be omitted with the linear regulator circuit. Instability will result if an IB pin capacitor is used.

2.5 Designing the Battery Voltage and -dV Detection Circuit

R9, R8:

R9 and R8 form the VAC (accumulator voltage) divider chain.

The VAC thresholds are:

0.3 V assume short circuit batteries. Trickle charge.
0.385 V minimum voltage for -dV detection.
3.85 V maximum voltage for -dV detection.
4.25 V assume open circuit batteries. Zero current.

R9 and R8 must be carefully chosen to keep the battery voltage within the -dV detection range, and to make sure that at open circuit the input voltage to the regulator is sufficient to cause an open circuit shutdown.

Table 2 lists appropriate values. These values apply equally well for all applications of TEA1100.

Table 2 VAC Divider Resistor R9, with R8 = 100 k

Number of cells	R9
2	10 k
3	47 k
4	100 k
5	150 k
6	180 k
7	220 k
8	270 k
9	330 k
10	390 k

C5:

Output capacitor C5 must be present (typically 100 µF or more) to stop rapid oscillation and LED flicker in the case of open circuit batteries.

2.6 Using the Temperature Protection Block

NTC input:

Where temperature protection is not required, the NTC pin (pin 3) can be tied to pin 10 or 11, reference current generator pins.

For connection of an NTC, see Application Note SPO/AN91007, page 37, 38, 45. The NTC circuit around pin 3 and calculations are correct for all applications of TEA1100.

2.7 TEA1100 Supply Connections

The voltage supply to TEA1100 should not exceed 12V. A supply decoupling RC filter should be applied to limit the voltage rise to $\leq 0.6V / \mu s$ at switch-on to ensure correct power-on reset. This filter also suppresses supply interference.

Where the DC input voltage to the circuit can exceed 12V, the supply to TEA1100 can either be voltage regulated or current-fed via a dropping series resistor.
A current supply to TEA1100 is allowed up to 15mA, while the IC internally zener clamps its supply voltage at 12V.

- Input supply voltage till 13V.

Apply at pin 12 a RC network R4 / C1: 68Ω / 330nF.
The operational DC input voltage range is between 5.9 and 13V.
At switch-on the unloaded input voltage should reach 6.7V to initialize TEA1100.

- Input supply voltage beyond 13V.

a) A 8V, 3-terminal positive regulator IC or a discrete series voltage limiter, (NPN transistor, zener, resistor) can be applied together with the decoupling filter R4 / C1.

b) TEA1100 supply adaptation can be simplified by using R4 as supply current-fed dropping resistor. R4 is determined by;

$$R4 = (Vin\ max - 12) / 15\ (k\Omega)$$ where Vin max is maximum average input voltage, not charge current loaded.

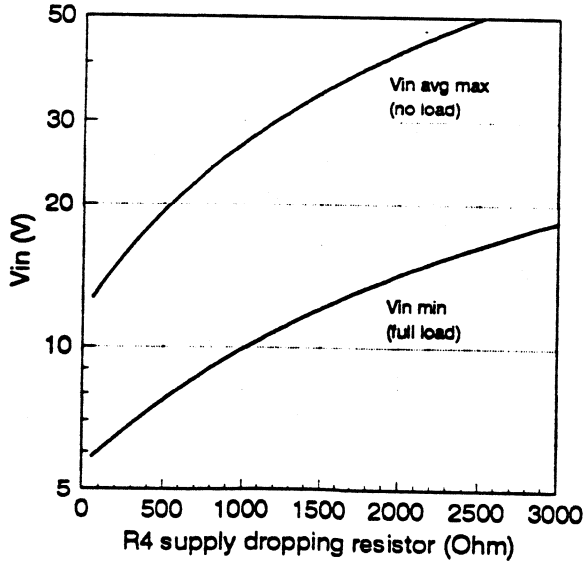
For continuous operation the loaded input voltage must not drop below;

$$Vin\ minimum = 4.3 \times R4(k\Omega) + 5.6V.$$

or else system reset might occur.

*) Note: If current-fed and input voltage >13V then via R5 and the LED, when not driven, additional unwanted current can be bypassed through the internal protection diode of pin 15 to the 12V zenered supply. To prevent this a resistor Rp can be added across the node R5 / LED anode and ground.
Resistor Rp value; $\leq 13 \times R5 / (Vin\ max - 13)$.

Input voltage limits with TEA1100 supply drop resistor.



3. MAINS INPUT

To use the linear regulator TEA1100 battery charger from mains requires an AC/DC convertor circuit. Either an existing power supply, a dedicated SMPS or low frequency transformer can be used.

The most simple low frequency transformer circuit is described here. The circuit consists of a step down transformer, a DC rectifier and reservoir capacitor. For economic design, the voltages and ratings of these parts must be chosen quite carefully.

A circuit diagram of the mains input section is shown in Fig 2.

The maximum charge current (Iout), and the number of cells to be charged must be known. The charge current is found from the battery capacity, and required fast charge time. A multiplying factor of 1.4 allows for the charge acceptance factor (which is less than unity) of the battery.

$$Iout = \frac{Ah \times 60 \times 1.4}{Charge\ Time\ (minutes)}$$

3.1 Reservoir Capacitor Values and Ratings

The minimum capacitor value required is calculated from Table 3 as the charger output current times the capacitance per ampere figure given. This gives the capacitor value for 30% ripple. The next larger value capacitor should be chosen. Using an excessively large capacitor value will cause a large ripple current to flow and is to be avoided. Smaller capacitors should not be used, as this could lead to the charger dropping out of regulation, leading to erratic performance.

The capacitor voltage ratings quoted in the table allow for 10% mains voltage variation, and 20% load regulation of the mains transformer. Also it is assumed that a transformer with the correct output voltage is used. If the load regulation of the mains transformer is greater than 20%, or a higher voltage transformer is used, then a higher voltage capacitor may be needed.

The ripple rating (in amps RMS) of the reservoir capacitor must be at least 2 times the maximum DC output current of the battery charger. Philips 056 series capacitors will prove suitable in most cases.

3.2 Transformer Voltages and Ratings

The VA rating of the mains transformer should be found as:

$$VA = 4 \times Iout\,(n + 1.5)$$

Where Iout is the output current of the regulator, and n is the number of cells.

This calculation assumes that the correct voltage mains transformer is used.

Overloading the mains transformer will lead to overheating and a possible fire hazard.

The secondary voltage of the mains transformer quoted in Table 3 is carefully chosen to allow for ±10% mains variation, diode drops in the circuit, and to keep power dissipation in the linear regulator to a minimum. Take care that the transformer is designed to give the recommended secondary voltage at maximum loading.

3.3 Rectifier Diode Ratings

The rectifier diodes must be chosen so that their I_F (av) rating is greater than the maximum output current, and that their V_{RRM} rating is at least equivalent to the DC voltage rating of the reservoir capacitor.

For up to 1 A, IN4001 are suitable, and up to 3 A, IN5401.

Table 3 Mains Input Section Components

Number of cells to be charged	Transformer secondary voltage V RMS, full load	Capacitor value µF / A	Capacitor voltage rating V DC
2	7.1	4000	16
3	9.1	3000	25
4	11.2	2400	25
5	13.2	2000	35
6	15.2	1700	35
7	17.3	1500	40
8	19.3	1300	40
9	21.2	1200	50
10	23.3	1100	50

For further details on TEA1100 please refer to Philips Semiconductors Notes NPO/AN9102 and SPO/AN91007.

4. DESIGN EXAMPLE

4.1 Design Specification

Charger requirement: 1 hour charger, 3 AA cells, UK mains input.

4.2 Design Procedure

Step 1. How much charge current is required?

$$Iout = \frac{Ah \times 60 \times 1.4}{Charge\ Time\ (minutes)}$$

To charge a 600 mAh battery in 1 hour or less requires typically:

$$Iout = \frac{600\ mAh \times 60 \times 1.4}{60} = 840\ mA$$

Step 2. Select mains components.

Transformer VA rating = 4 × Iout × (n+1.5) = 4 × 0.84A × (3+1.5) = 15 VA

Transformer primary voltage = 240 V RMS

Transformer secondary voltage (from Table 3) = 9.1 V RMS, full load.

Reservoir capacitor value (from Table 3) = 3000 µF / A × 0.84 A = 2520 µF

Next larger capacitor = 3300 µF

Reservoir capacitor voltage (from Table 3) = 25 V

Reservoir capacitor ripple rating = 2 × Iout = 2 × 840 mA = 1680 mA

Chosen capacitor: Philips 056 series type 2222 056 56332

NB: Check ripple rating.

Rectifier diodes: IN4001

Step 3. Select regulating transistor and driver.

Using Table 1:

T1 = BDT60A, T2 = BC635, D1 = IN4001, R2 = 180R

Step 4. Calculate heatsink size.

The maximum power dissipation in the series pass transistor will be:

Pdiss = 1.30 × Iout × (V sec - 2.0)

where V sec is the RMS AC secondary voltage of the mains transformer, from Table 3.

Pdiss = 1.30 × 0.84 × (9.1 - 2.0) = 7.8 W

for a maximum temperature rise of 55 °C, the required heatsink size is:

55 °C / 7.8 W = 7.0 °C / W

Step 5. Evaluate viability.

Having completed steps 1 to 5, all the major cost and size determining items in the circuit have been specified. From this it can be decided whether or not the linear regulator is suitable, or whether a switch mode solution is required.

Step 6. Setting the charge currents.

Starting with R6 = 27 k,

Choose R1 to give between 50 and 200 mV.

For 840 mA, a value of R1 = 0R1 will give a voltage of 84 mV, inside the desired range.
R1 = 0R1

$$R3 = \frac{R6 \times R1 \times Ifast}{1.25}$$

$$R3 = \frac{27k \times 0R1 \times 0.84}{1.25} = 1814R = 1k8$$

Trickle charge is chosen as one twentieth Ifast, hence prescaler factor = 1 with R7 open. Therefore PR connected to Vsource.

Trickle charge current = 42 mA

Step 7. Setting system timings.

Time out can be set at 60 minutes.

R6 = 27 k, p = 1

$$C3 = \frac{60 \times Time\,Out\ (minutes)}{0.93 \times R6 \times p \times 2^{26}}$$

$$C3 = \frac{60 \times 60}{0.93 \times 27000 \times 1 \times 67108864} = 2n2$$

Step 8. Battery voltage and -dV detection circuit.

From Table 2, R8 and R9 are chosen.

With n = 3, R8 = 100 k, R9 = 47 k

Step 9. Voltage Regulator bias.

R11 is chosen for a minimum of 0.2 mA in Zener D3. Minimum input voltage is 10 V, therefore R11 = 0.9 V / 0.2 mA = 4k7.

Table 4 List of Parts, Linear Regulator Design Example

R1	0R1
R2	180R
R3	1k8
R4	link
R5	2k2
R6	27 k
R7	open
R8	100 k
R9	47 k
R10	1 k
R11	4k7
C1	open
C2	10 nF
C3	2n2
C4	-
C5	100 µ, 25 V
C6	10 n
D1	IN4001
D2	3 mm LED
D3	BZX79C9V1
T1	BDT60A
T2	BC635
T3	BC549
IC1	TEA1100

Table 5 List of Parts, Mains Input Section Design Example

TR1	240 V primary, 9.1 V secondary, 9 VA
D1-D4	IN4001
C1	3300 µ, 25 V Philips 056 series
F1	500 mA fast blow

Table 6 List of Parts, Linear Regulator Section

R1	See Section 2.3
R2	100R / 180R. See Section 2.1
R3	See Section 2.3
R4	68R. See Section 2.7
R5	2k2
R6	See Section 2.3
R7	See Section 2.3
R8	100 k
R9	See Table 2 and Section 2.5
R10	1 k
R11	See Section 2.7
C1	330 n. See Section 2.7
C2	10 n. See Section 2.4
C3	See Section 2.2
C4	-
C5	100 µ DC voltage as mains reservoir capacitor. See Section 2.5
C6	10 n. See Section 2.7
D1	IN4001/IN5401. See Section 2.1
D2	3 mm LED
D3	9V1 Zener. See Section 2.7
T1	BD132/BDT60A. See Section 2.1
T2	BC549/BC635. See Section 2.1
T3	BC549. See Section 2.7
IC1	TEA1100/TEA1100T

Table 7 List of Parts, Mains Input Section

TR1	Mains transformer. See Section 3.2
D1-D4	Rectifier diodes. See Section 3.3
C1	Reservoir capacitor. See Table 3, Section 3.1
F1	500 mA fast blow

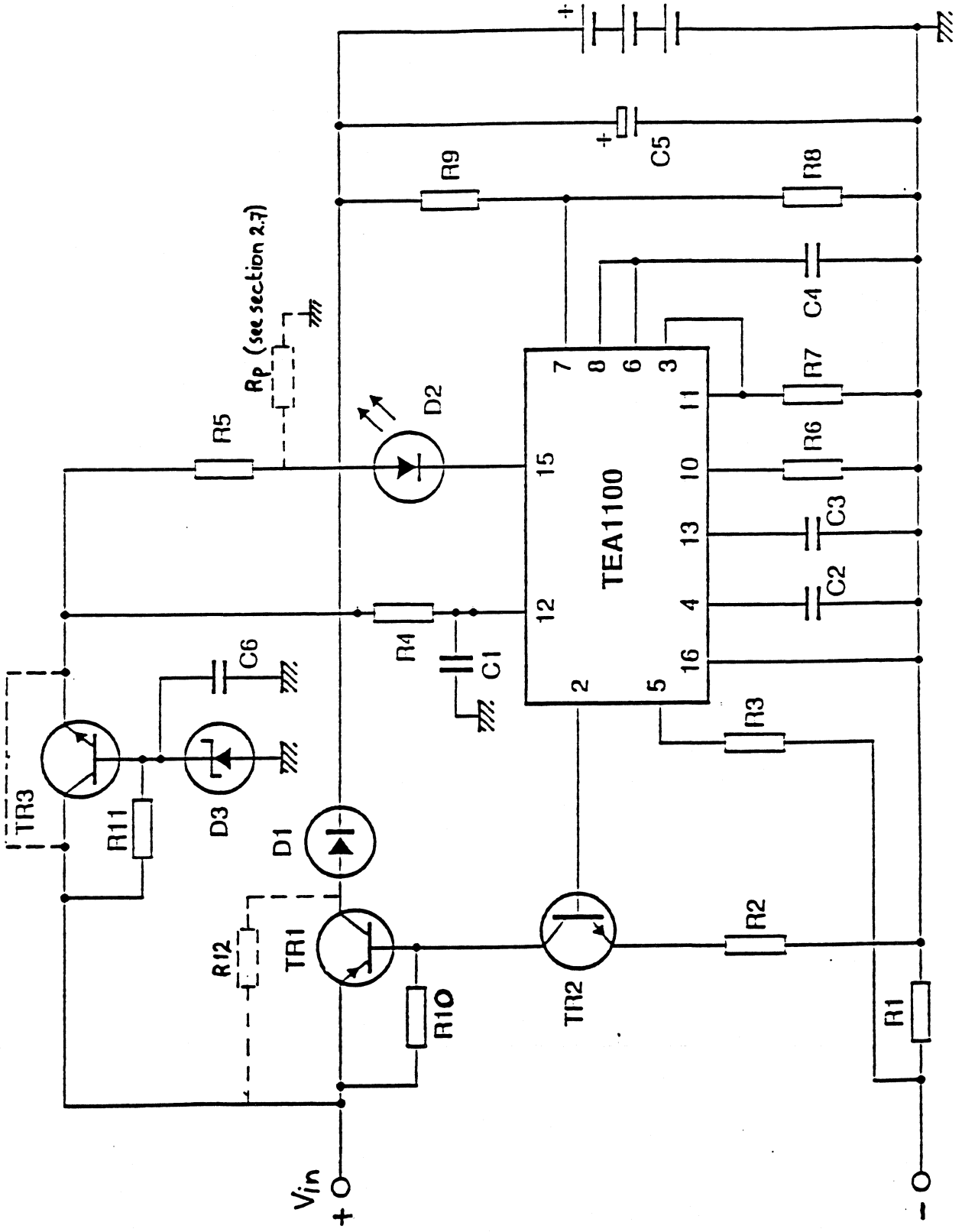


Fig 1 TEA1100 Battery Charger with Linear Regulator Circuit

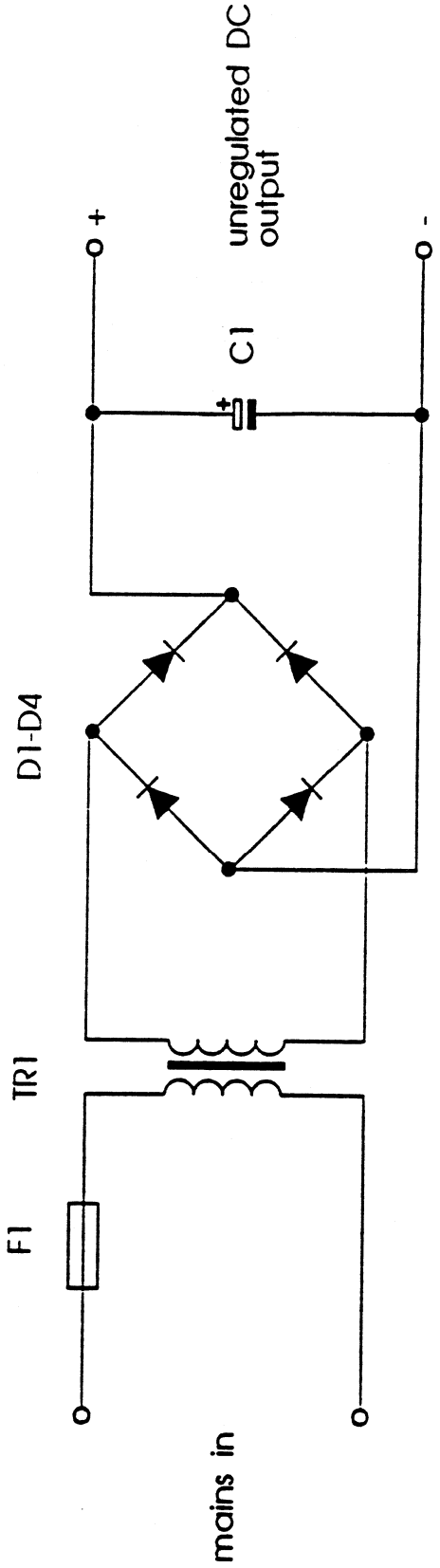


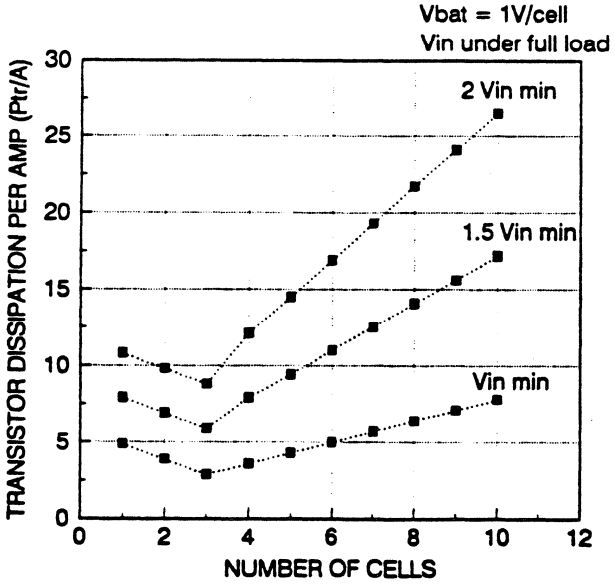
Fig 2 Mains Input Circuit

Appendix 1

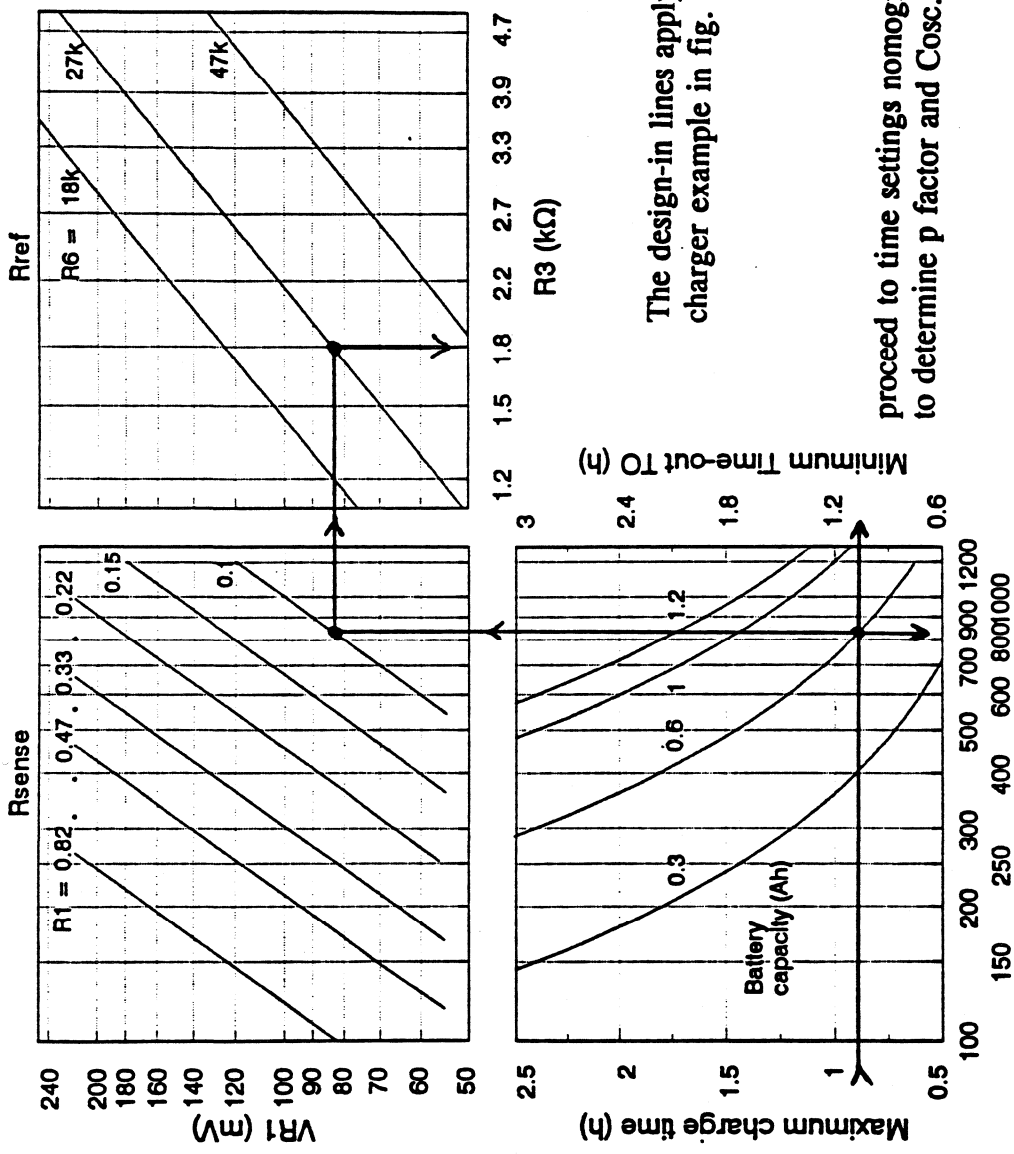
Survey of settings for 1 - 10 battery cells application.

		Vcell max = 1.7V			T1;Vce sat max = 0.8V			Vd1 max = 0.9V			
number of cells		1	2	3	4	5	6	7	8	9	10
D1 required		no	no	no	yes	yes	yes	yes	yes	yes	yes
Vin min - full load	V	5.9	5.9	5.9	8.5	10.2	11.9	13.6	15.3	17	18.7
Vin min - no load	V	5.9	5.9	5.9	8.7	10.4	13.	14.9	17.2	19.7	22.5
Vin avg max - no load	V	13	13	13	20	27	30	39	45	45	53
Vbat max (Ifast)	V	1.7	3.4	5.1	6.8	8.5	10.2	11.9	13.6	15.3	17
Vbat full (Itr)	V	1.4	2.8	4.1	5.5	6.9	8.3	9.7	11.	12.4	13.8
Vbat high prot.=>	V	4.3	4.3	5.7	7.7	10.6	11.9	13.6	15.7	18.3	20.8
Vbat low prot.=<	V	0.3	0.3	0.4	0.55	0.75	0.84	0.96	1.11	1.29	1.47
R4 (supply)	Ω	68	68	68	560	1000	1200	1800	2200	2200	2700
R12 (Rshunt)	kΩ	10	8.2	8.2	15	18	22	27	33	33	39
R8 (Rvac-)	kΩ			100	100	100	100	100	100	100	100
R9 (Rvac+)	kΩ	12	12	33	82	150	180	220	270	330	390

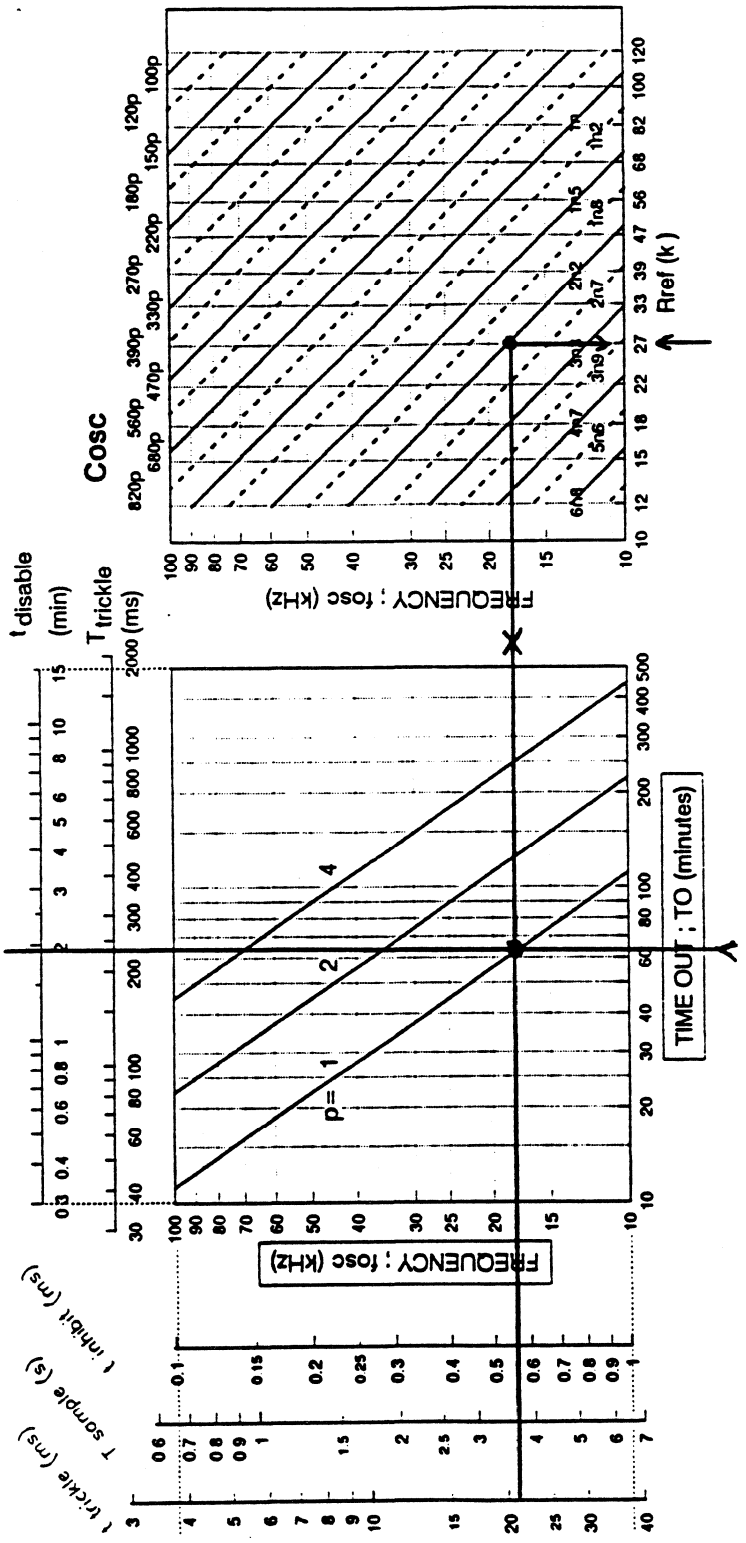
Dissipation in regulator power transistor.



Appendix 2



NOMOGRAM OF CHARGE CURRENT SETTING WITH TEA1100



NOMOGRAM OF TIME SETTINGS IN TEA1100

APPLICATION NOTE

ICs for Battery Management

TEA1100
Versatile battery management IC for NiCd charge systems

Report No: NPO/AN9102b

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Customer & Product Support Group Consumer ICs Nijmegen, the Netherlands.

Keywords
Power Control & Misc.
Battery management
NiCd/NiMH fast charger
TEA1100

Date : 04-11-1992
Pages: 33

SUMMARY:

The TEA1100 is a battery management circuit intended for fast and very fast charging of Ni-Cd batteries. The I.C. detects full charge by means of - V and it incorporates temperature and time-out overcharge protections. The I.C. can control either a d.c. or switched mode power supply directly.
The IC is versatile in use and can be applied for a wide range of charge requirements.
This note is intented as an initial users guide to support the introduction of TEA1100.

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1. INTRODUCTION

Rechargeable Ni-Cd batteries are undoubtedly becoming the common standard power source in portable electric and electronic appliances. Not only are Ni-Cd batteries advantageous economically and environmentally compared to throw away batteries, but they are essential in the expanding market of power equipment.
Obviously connected with rechargeable batteries is the need for charging units. As wide as the application areas for Ni-Cd batteries are; from stand-by low power use to heavy power tools, so too are the criteria for recharging methods. Similarity in requirement aspects are; reliabilty, long life time, high number of recharging cycles and of course low cost.

The complexity of the charger unit will increase with demand for shorter charge time and higher charge capacity cells. Charge rates presently vary from 0.1C normal recharge up to 4C ultra fast recharge with cell capacity ranging between 0.5 and 4 AHr.
Therefore the power needed from a fast charge supply unit will in most cases reach such a magnitude that switch mode conversion is the only solution to reach an acceptable efficiency and volume.

For charging systems, especially quick charge up to ultra fast charge, we have designed a management I.C. TEA1100, which monitors and controls charge in the Ni-Cd batteries under recharge. This I.C. offers great versatility and design freedom which, in combination with a charge supply, can ease the designers task to realise the optimum system with a minimum of engineering time.

The most important features of TEA1100 are;

- Accurate detection of fully charged batteries using -dV sensing.
- Adjustable absolute maximum fast charge period.
- Adjustable pulsating trickle charge with full batteries.
- Temperature guarding and out of range voltage protection.
- Charge current regulation control for a charge supply (e.g.SMPS).

A full listing of features can be found in table 1.

This paper gives a summary of existing charge methods with charge rate capacity as a review for the applied charge approach in TEA1100 and its charge regime.
Further on, design orientated functionallity and characteristics of TEA1100 will be explained with ideas for circuit design. Finally, a design example of a 12V input fast charge system is described.

2. CHARGING METHODS.

The nominal charging rate for batteries is 0.1C, at which it requires about 14 hours to fully recharge flat batteries. This charge rate is harmless when maintained for a far longer period as no considerable heat or pressure rise will occur in the batteries. Although safe, continuously applied normal charge will result in degradation of the battery's maximum attainable life time. Therefore very long overcharge should be limited by switch off or switch over to a lower rate only required to counteract the worst case self discharge in the batteries.

For all charging rates above normal charge it is necessary that the charge progress is controlled. The methods used vary from timing control, (the simplest but not the optimum manner with quick charge) to a combination of time, temperature and voltage control with very fast charge. When the batteries reach full charge then the charge rate must be reduced to a safe trickle charge level otherwise overheating will occur with danger of venting cells or even explosion (very fast charge).

Figure 1 shows the different charge cutoff methods.

a) Time control is a safeguard against too long an overcharge period. It is the simplest applicable method but it is static and does not take into account the state of charge of the batteries. For maximum battery life the use of this cutoff alone at rates up to quick charge (0.3C) is not optimal and is certainly unsuitable at higher charge rates.

b) Temperature rise indicates full batteries when the charge energy is no longer stored but being dissipated in the cells. It is measured by a thermistor close to the batteries. The response time of this sensing is relatively slow and also ambient temperature affects the outcome. This method can be used at charge rates between quick and fast charge (<1.5C).

c) Absolute maximum voltage control is too complex. The battery sense voltage needs a type of temperature compensation but the changing level of the charge voltage profile of the battery during its lifetime is unpredictable .
This cutoff method is not recommended.

d) Relative voltage control using the -ΔV principle has long been proven to be a very reliable cutoff method. It makes use of the characteristic phenomenom that the battery voltage drops slightly when the inside temperature increases due to the nearly fully charged condition. Compared to outside temperature control this method is direct with a fast response and therefore it is the better method with fast charge and the only reliable cutoff approach with very fast charge.
The drawback of this method has been the complexity in the realisation of a very secure and sensitive -ΔV detector.

With all the cutoff methods mentioned above it is essential that the current supply is sufficiently constant neither to interfere with the charge time nor to cause battery voltage fluctuation under sense.

3. CUTOFF CONTROL AND CHARGE REGIME WITH TEA1100

3.1 Cutoff methods

The main cutoff principle in TEA1100 is -ΔV detection. This method has been proven to be reliable and applicable over a wide range of charge rates. It is also based on design experience of such a detector and its practical use.

The detector features a currentless wide input voltage range which adapts, with or without an additional resistive divider, to any number of fixed cells or a variable range of cells.
The detection is related to the top voltage level of the batteries and therefore independent of the absolute battery voltage. Detection occurs when the battery voltage drops 1% below its maximum recorded value.

The second cutoff method incorporated as a safety guard is time out; a wide maximum charge period setting for the rare case of no -ΔV occurrence.(faulty batteries).

3.2 Protections

TEA1100 contains conditional protective charge control circuits;

For fast charge release the battery voltage must be within a certain range. In case of a too low battery voltage, reconditioning of the batteries will be attempted with trickle charge. When the voltage happens to be too high it is seen as a non connected battery which stops and resets system operation, followed by restart.

The second optional protection is under and over temperature, measured via a thermistor on the battery. This protection prevents fast charge when the battery temperature is outside a specific range which is safe for the applied battery type (10°- 45°C typical).
Outside that range the trickle charge mode will take over as a high charge rate will certainly damage the batteries.
A too high battery temperature can indicate that the cells have been under strain in use, for instance by high discharge. Directly trying to recharge excessively hot batteries will then only occur at trickle charge, allowing the batteries to cool down. When thereafter fast charge takes over, the battery temperature will drop even faster due to the endothermic effect.
If temperature protection occurs within a charge session then the timing state is set on hold while the voltage monitor is reset.

3.3 Charge system characteristics

With TEA1100 linked as the control stage to the charge current supply, the system performance obtained is shown by the state diagram in figure 2.

4. TEA1100 FUNCTIONAL BLOCKS AND USE

This section explains the functional blocks of TEA1100.
For design in, useful characteristics will be given as far as it is not detailed in the data specification. The adjustable parameters receive full attention and system approaches are indicated with simplified diagrams.

For the terminology of the I.C.s' input, output and program pins, reference can be made to the list with figure 3.

As shown in figure 3, TEA1100 consists of the following blocks;

1. Supply
2. Monitor
3. Timing
4. Protection
5. Regulation control

4.1. The supply block

This block provides bandgap stabilised voltages for all circuitry and outputs 1.25V at Rref and 4.25V at Vsource.
Nearly all adjustable features of the I.C. are related to currents which are drawn from the Rref voltage. The output current from Rref to common, via a resistor, is the basic reference. Vsource makes a reference supply for external use.
The supply input Vs is provided with an under voltage lockout with hysteresis while the maximum voltage is zener protected. The graph in figure 4 gives supply characteristics under various operating modes.
At initialisation a reset pulse is generated for all the internal logic.

4.2 The monitor block

The monitor tracks the (divided) battery voltage over a wide input voltage range, 0.38- 3.8V, and it makes the decision when the batteries are fully charged. When that occurs it will trigger the permenant switch-over from fast charge to trickle charge. Fast charge can then only resume following a reset.
From a very high impedance sense input, VAC, the monitor receives the "battery" voltage via a filter and a sample and hold circuit. The repetitively sampled sense voltage is a/d converted and the digital output value is then compared with the previously stored value in the register. The register value will and can only be replaced by a new, higher value. When subsequent sampled values decline because of battery voltage drop (fully charged), then those values are compared with the last maximum stored. If a measured value is ≥1% below the maximum stored, then the monitor's last remaining action is to set the trickle charge mode.

False voltage sampling must be avoided. It could be caused by fluctuation or interference on the charge current, bad battery connection, shock or

vibration. The safest method of sampling is to interrupt charge during the sampling interval. This is realised by an inhibit signal on all the outputs for supply control use. Within the inhibit period the charge current should decay to zero so that at the end of this period sampling of currentless battery voltage takes place.
At the beginning of the charge session, the sample and hold will already be active. The monitor however, only starts recording after a certain time, **the disable time**, has elapsed. This period allows the battery to format or recondition.

The required clock and control pulses are directed by the timing block and the designer has to reckon with the settings of;

- disable period
- sample rate and duration
- charge supply inhibit during sampling

The time setting formulae are given in the timing block section 4.3.

The direct output of the monitor block is the **LED** pin. This pin is grounded when charge is enabled and floats when not. This signal can be used as on/off remote control for a stand alone charge supply.
The LED signal can also be mixed externally with a current reference signal from the control block to provide a 3 state control signal for the supply;

- on and high current reference ; fast charge
- on and lower current reference; trickle charge
- off

It requires an interface to adapt the reference signals to the current reference control stage of the supply.
A block configuration of this suggestion is shown in figure 5.

4.3. The timing block

This block is the operating heart of the IC. All the timing signals are extracted from a counter control stage which receives its clock signal via a prescaler from the oscillator. Therefore the timing signals are proportional to the oscillator period time, **Tosc** and the prescale factor.
The prescaler with its programmable dividing factor **p** = 1, 2 or 4 presets the ratio between fast and trickle charge rates. For a required oscillator frequency setting to be used for SMPS control, the p factor setting can be used to adjust the maximum fast charge time (**TO**) to an acceptable value.

In the trickle charge mode, an on/off timing signal is sent to all the output stages so that charge supply operation is pulsating. During the on and off periods the maximum IC supply current requirement characteristics are 4.1mA and 1.7mA respectively.(Fig.4).
If a charge light indicator is used, e.g. a LED, then the trickle charge repetition time should be longer than 20ms to ensure that light flashing remains visible. If necessary the trickle or LED repetition time can be scaled down by adjustment of the prescaler p factor.

A LED can be connected at the supply output or driven via the LED pin. The time settings and formulae are as follows;

- Oscillator frequency is set by;
  the current out of Rref with a resistor to common, 13k< R< 130k,
  and the capacitor on the OSC pin by; **Tosc= 0.93 x Rref x Cosc**

- Absolute maximum fast charge period; **t_{TO}= 2^{26} x p x Tosc**

- Scale factor p is set by PR on Vsource, open or common for resp. p= 1,2 or 4.

- Monitor disable period at begin of fast charge;
  t disable= 2^{-5} x TO

- Monitor sampling repetition time; **t sample = 2^{16} x Tosc**

- Monitor sampling inhibit period; **t inhibit= 10 x Tosc**

- Monitor sampling actually takes place at the tenth oscillator cycle during t inhibit.

- trickle charge repetition time; **T trickle= 2^{12} x p x Tosc**

- Trickle charge on duration; **t trickle= 3/4 x 2^{9} x Tosc**

4.4 The protection block

The functionality of this block is already described in section 3.2, protective control circuits.

4.5 The regulation control block

This block provides additional control and consists of current control circuitry for a direct current or a switch mode power supply. These circuits are an error amp followed by both a Pulse Width Modulator and an analog amplifier, AO.
The circuits will be described in relation with the diagram in figure 6 and the waveforms in figure 7. For a current supply the flyback converter is taken as example.
Charge current is the demagnetising current of the transformer during the flyback stroke of the SMPS. Since the minus battery pole is connected to the ground of TEA1100, the sawtooth voltage pulses across the sense resistor Rs are negative going with respect to ground. The voltage pulses are averaged via the RC network, R1 and C1, and shifted positive to ground level by passing a reference current from the Ib pin through R1.
The Ib reference current can take two values during the charge cycle;

a) the current Iref, set via the Rref pin, internally activated in the fast charge mode;

$$Iref = 1.25V / Rref \qquad (10\mu A < Iref < 100\mu A)$$

b) the current In, set via the Rn pin, internally activated in the trickle charge mode;

$$In = 1.25V / Rn \qquad (5\mu A < In < 50\mu A)$$

or in default of Rn; $In = 0.5 \times Iref$

The error amp +input Ib refers to ground level. This amplifier has a forward transconductance characteristic which is given in figure 8 and its gain and phase response in figure 9.
In the linear operation range $g_M = 250\mu A/V$ at V_{Ib} within ± 50mV.
The output connection is the LS pin. Output saturation current is ±20μA at V_{Ib} > ± 150mV and the output voltage range is between 0.5 and 3.6V.
These characteristics are important design items for correct current sensing, loop response and stabilisation.

The current sense input network must be carefully choosen.
The sense resistor Rs will be chosen as small as possible power wise, but the average voltage must be large compared to the reference tolerance; ±5mV.
The R1,C1 time constant should not be too long (response time) but sufficient to ensure that the residual ripple on the averaged sense voltage is < ±100mV in worst case. Only then will the average charge current be correctly represented at the error amp output through lineair operation.

The fast charge current is set by;

$$Ich = \frac{Iref \times R1}{Rs}$$

The average trickle charge current is set by;

$$Ich = \frac{In \times R1}{Rs} \times \frac{0.094}{p}$$

(where the last term states the charge current duty factor)

On the LS output a capacitor, possibly with a series resistor, must be connected to ground to obtain the required feedback error voltage. *)
The output load network adds compensation to the small signal loop. In table 2, given with figure 9, compensation circuits with resulting gain response are shown and an example is plotted in figure 9.

The error amp output contains a series switch which is open during both the monitor inhibit period and the trickle charge off period. In these periods the charge current interrupts causing the error amp output to go high. The feedback regulation voltage, present before those interrupts, remains stored by the LS capacitor due to the open switch. When charging resumes, the current will quickly stabilise at its regulation level with

*) Note: A resistor on LS to ground, e.g. an 1MΩ probe, causes an input offset dependent on the output voltage according to: Vin= Vout/ 250μA x Rload. So at Vout= 2V, 1MΩ gives 8mV offset.

minimum current overshoot.
At initialisation or after a protection occurence a slow start is also achieved by the LS capacitor which at protection is discharged via the LS pin to ground. Figure 10 shows the start cycle.

The error amp output can be used via a buffer, the analog output AO.
The voltage gain of this amplifier is 4x (12dB) with a gain bandwidth of 4MHz. The transfer characteristics are shown in figure 11.
By means of current programming at the CP pin the amplifier can be set either inverting or non inverting with respectively a sink or source output.

AO; non invert; CP pin left open
invert; CP pin via R=56kΩ to ground

The AO output can be used to control a dc supply or a stand alone SMPS where an optocoupler is used for mains isolation .

For duty cycle regulation the error amp output is passed to the pulse width modulator PWM. The error voltage is the slicing level which is compared with the oscillator waveform to produce rectangular pulses as shown in figure 12.
Via a latch, only one pulse per cycle starting in the oscillator flyback is enabled as output (anti-multiple pulsing).

The error voltage can be modulated with the supply current waveform. See figures 13 and 14. This type of current control or feed forward adds cycle by cycle regulation to the relatively slow loop regulation. This enhances the response to sudden changes in supply operation with minimum current overshoots. Modulation can be achieved via the LS capacitor which instead of being grounded is connected to a negative going sense voltage of the duty switching current (flyback and forward SMPS).
It can also be achieved via the error amp by means of a resistor R_{LS} in series with the LS capacitor (forward SMPS only). By this manner the sense voltage at the error amp input should not be filtered while the ac ripple voltage must be well within the linear input voltage range. The added modulation voltage on LS is 250μA x R_{LS} x Vi, and it reflects the ac current waveform and partly an error in the dc supply current. Together with a relatively small C_{LS} fast tracking of the dc loop is realised.

Similar to the analog output the polarity of the PWM output pulses can be inverted by current programming at the CP pin. In either mode the output can sink or source current.

In the trickle charge off period auxillary output pulses can be produced, programmed by the CP pin . These pulses have a 14% duty factor and a repetition rate of Tosc x 8. They are intended to support primary and secondary supply recovery in an isolated supply.

non invert; CP pin via R=120kΩ to ground
invert; CP pin via R= 22kΩ to ground

The PWM output can be used to control the drive of a SMPS switching device directly or a mains isolated supply via a pulse transformer (master-slave principle).

5. EVALUATION BOARD OF A DC/DC SMPS CHARGER

An experimental design of a 40 minute charger is shown in figure 15. The circuit applies TEA1100 in combination with a low voltage forward converter switching at 40kHz. This system will charge a maximum of four, fast charge type, AA cells (550mAHr) from a dc input voltage between 11 and 16V. The fast charge rate is 2C while the trickle charge rate is 0.05C by means of 550mA current bursts.
The board layout is shown in figure 16.

5.1 Design specification

Fast charge current: 1.1A.
Trickle charge current: ≈28mA.
Output overvoltage protection: < 9V.
Max. cell voltage under charge: 1.7V.
Abs. max. charge time: 45- 60min.
Trickle repetition time: ≥ 80ms.

5.2 Circuit description

The main parts of the forward converter are the swiching device T1, the flywheel diode D2 and the choke L1 in series with the battery load. The switch is driven by transistor T2 which receives duty cycle controlled pulses from the control circuit TEA1100. The supply is current regulated and TEA1100 senses the current at resistor R4.
The battery voltage is continuously monitored via divider R14,R15 and temperature guarded via divider R11,R_{NTC}. The charge mode is indicated by a LED, D5, which is on continuously during fast charge and flashes during trickle charge.
The network with T3 adapts the supply input to the I.C. supply.
The residual components around the I.C. program the timing control, the charge current and its regulation.

5.3. SMPS operation and coil design

5.3.1. Operating limits

The forward converter regulation equation is; $Vo' = \delta\ Vi'$

where: Vo'= the voltage across L during the off time of T1 and hence
$Vo' = Vbattery + V_F(d2) + V_{R4}$.

Vi'= the supply voltage at L during the on time of T1 and hence
$Vi' = Vs - V_F(D1) - Vsat(T1) - V_{R4}$.
δ = duty factor ton/T; TEA1100 δ cycle range= 0 to 80%.

The limits in supply operation are;

a) maximum Vi' and minimum Vo' e.g. battery short (trickle charge).
At this condition the δ cycle is minimal and is 6%.

b) minimum Vi' and maximum Vo' when the battery is nearly fully charged
The maximum δ cycle restricts the last condition so if taken;
maximum battery voltage at end of charge= 4x1.7V= 6.8V,
V_F of the diodes D1,D2 $\leq$0.8V , Vsat of T1 $\leq$0.4V and VR4= 0.28V then the min. input voltage Vs= $\leq$10.9V.

5.3.2. Determination of the coil

The maximum inductance is limited by the requirement that the maximum inductance current must decay to zero within 9 period cycles (monitor sense inhibit period). The worst case condition is at minimum Vo' which is assumed to be 4 x 1V= 4V; the reconditioned low battery voltage.
By approximation;

$$Lmax = 9\ Tosc\ (Vo + V_F)\ /\ Io :$$
$$Lmax = 9x25x10^{-6}x4.8\ /1.1 \approx 980\mu H.$$

The minimum inductance is limited by the condition of continuous coil current flow. The worst case situation is the maximum ripple current at the lower output current setting (i.e. trickle charge). Maximum ripple ΔI_L equals 2xIaverage (=1.1A) and this occurs at Vo_{max} with 50% δ cycle.

So according to;

$$Lmin = Vo'max(1-\delta)T\ /\ 2Iav :$$
$$Lmin = 7.6x0.5x25x10^{-6}/\ 2x0.55 \approx 87\mu H.$$

A compromise has to be chosen between the switching peak current I_{Lmax}, the core size determining I^2L value and the current deviation rate with respect to loop response.

The chosen inductance value is: L= 400μH.

and now derived; ΔI_L max = 238mA
I_L peak= 1.1 + 0.238/2$\approx$ 1.22A

The abs. max. peak current is taken on the safe side: 1.25xI_L peak $\approx$1.5A.

- For the core a RM type is selected by;

  Abs max energy: $I^2L = 1.5^2x400x10^{-6} \approx 0.9mJ$
  Derived from core data the core choice is;
  RM7/i, 3C85 grade , airgap= 0.4mm

- The winding number of turns and wire size are;

  with a 0.4mm airgap the inductance per turn is; $A_L \approx 160nH$
  so the winding number of turns becomes; $N = (L/\ AL)^{1/2} \approx 50$

  and the wire size required is AWG 27 ($\approx$0.35mm).

5.4. Control I.C. TEA1100 and its associated components

The peripheral components for TEA1100 will be specified by function and design order.
For settings and formulae see also sections 4.3 and 4.5.

Pin 10; Ireference setting via R13. Chosen current is 46μA so; R13=1.25V/46μA= 27kΩ. This current equals the reference current for fast charge regulation.

Pin 11; I_N reference current for trickle charge regulation. The default value 0.5xIref is chosen so this pin can be left open.

Pin 13; Oscillator. The frequency is set by C7 and the reference resistor at pin 10. For Tosc= 25μs; C7= 25μs/ 0.93x27k $\approx$ 1nF.

Pin 8; p scaling factor. By leaving pin 8 open, p is set for a factor 2 to obtain an abs. max. charge time $_{TO}$ of 2^{26}x2x25μs $\approx$ 56minutes which is required.
(With pin 8 connected to pin 6, p= 1 and TO will be 28minutes and with pin 8 to ground then p= 4 and TO becomes 112minutes).

All the other timings can now be derived;

Trickle charge:	T trickle= 0.2s	
	t trickle= 10ms	; hence: δ factor= 5%.
Monitor part:	t disable$\approx$ 1.7min	
	T inhibit$\approx$ 1.6s	
	t inhibit= 250μs	

Pin 7; Monitor input. The input voltage is adapted to the battery voltage by divider R14,R15. A divider factor 0.5 is taken which results in battery overvoltage and max. - V detecting voltage levels of 8.5V and 7.7V respectivily.

Pin 3; Temperature protection input.
From a constant bias voltage source the divider R11, R_{NTC} adapts the batteries safe temperature range with the input voltage window of pin 3.

In appendix 3 a calculation procedure is given for the determination of the NTC network.

If temperature sensing is not used then R11 is omitted and pin 3 should be connected to pin 11.

Pin 5; Current sense input. The resistors R4, R8 and the reference currents I_F and I_N determine the charge current regulation levels. For a fast charge current= 1.1A, I_F= 46μA and R4= 0.25Ω then;

$$R8 = 1.1 \times 0.25 / 46 \times 10^{-6} \approx 6k;\quad 6k2 \text{ taken.}$$

With the given I_L max.= 0.23A the maximum ripple voltage at pin 5 becomes: 0.23xR4= 58mV.

C5 is small and only present for hf noise filtering.

Pin 4; Loop stability. The functions achieved via this pin are; error control voltage retrieval and frequency bandwidth setting with C6 and error voltage modulation with inductance current information via R9.
C6= 680pF. This value is as small as possible. Its residual ripple p-p voltage, 90°phase lag with the input voltage, is at most 70mV.

The ac modulation voltage across R9= 47k becomes maximum;

$$V_{R9} = 250\mu \times V_{in} \times R9 = 0.68Vp\text{-}p.$$

Pin 9; Change polarity. The polarity of the duty cyle output pulses at pin 1 have to be positive. This is set by leaving pin 9 open. (A reversed polarity is set with a 56k resistor at pin 9 to ground).

Pin 15; LED output. This pin is used to switch on a LED when charge is supplied. The trickle charge mode is indicated by a flashing LED.

Pin 12; IC supply. The supply is derived from the input voltage via a voltage clamp circuit with T3 and D4. The low impedance of this circuit together with C4 prevents IC supply on/off oscillation within the low supply cutoff hysteresis band at initialisation.

Pins not used;

Pin 2 ; Analog output.
Pin 14; Synch.

6. SUBSEQUENT APPLICATION EXAMPLES

In appendix 4 some circuit design ideas are given for application of power Mosfets as SMPS switching devices.
Also given is a dc regulated charge source in case a switch mode power source is not acceptable because of interference. This dc charger with TEA1100 is the simplest of its kind.

Application notes which can be expected soon will give description of battery management systems which apply the flyback converter topology.
The system examples are;

a) a charger with low supply voltage input, 12V, capable of charging 6 AA type cells in one hour. The output can easily be adapted for other requirements.
b) a charger with world wide mains input, 90 - 265V, providing mains isolated output. It can charge a battery pack containing 8 cells with 1.5AHr capacity within one hour.

TABLE 1 TEA1100 FEATURES

TEA1100 Battery Management Systems

Application

* Monitor and Control circuit for NiCd charger systems

Features

* Accurate detection of fully charged batteries using -ΔV sensing, with 12.5 bit resolution, digital filtering, currentless voltage sensing, and nominal -1% (w.r.t. to top level) -ΔV detection level.
* Adjustable Time-Out of fast charging, -ΔV detection inhibited for the first 3.1% of Time-Out.
* Tracking of Time-Out with charge rate.
* Switch over to trickle charge following either -ΔV detection or Time-Out.
* Pulsating trickle charge current with 10, 5 or 2.5% duty factor setting to avoid cell degradation due to dendritic grows.
* Detection of low battery voltage, during which time trickle charge is applied, and timing reset.
* Protection against open circuit batteries, during which time outputs are switched off, and timing reset.
* Charge current regulation in conjunction with a SMPS via Analog and PWM outputs.
* Temperature guarding possibility by means of NTC resistor. Outside set temperature range, trickle charge takes place. Hysteresis is built in to avoid rapid on/off cycling.
* Independently adjustable ratio between fast and trickle charge rates, ratio range 10 to >500, set by two external resistors and duty factor selection.
  Default trickle rate=1/20 fast rate (d=10%) if only one resistor is used.
* Large 10:1 voltage range of operation of -ΔV circuit.
* 16 pin DIL package.

Fig.1a TIMER CUTOFF

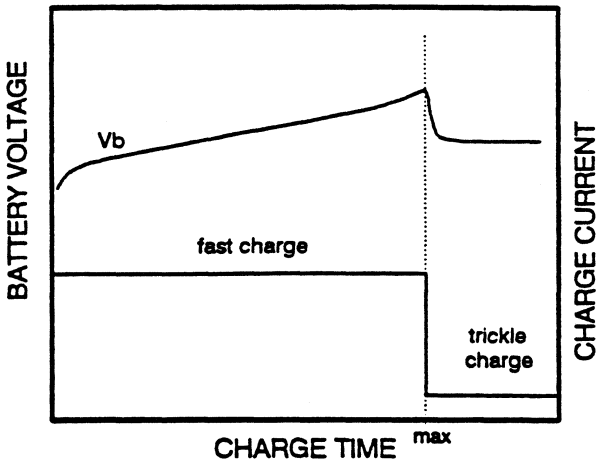


Fig.1b TEMPERATURE CUTOFF

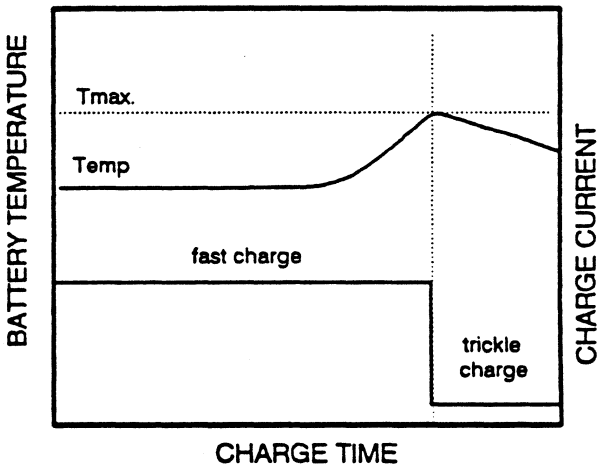


Fig.1c MINUS DELTA VOLTAGE CUTOFF

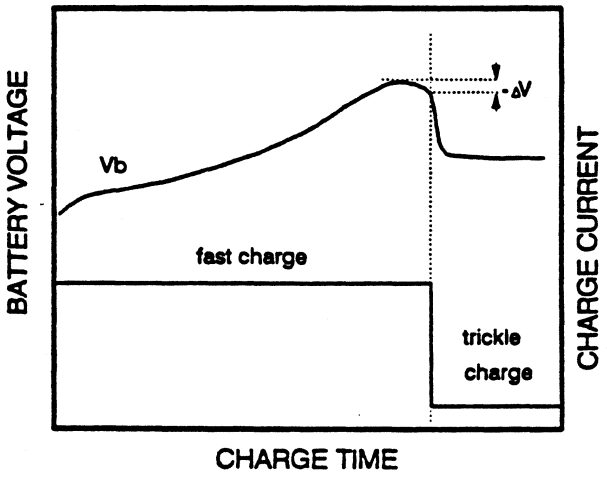
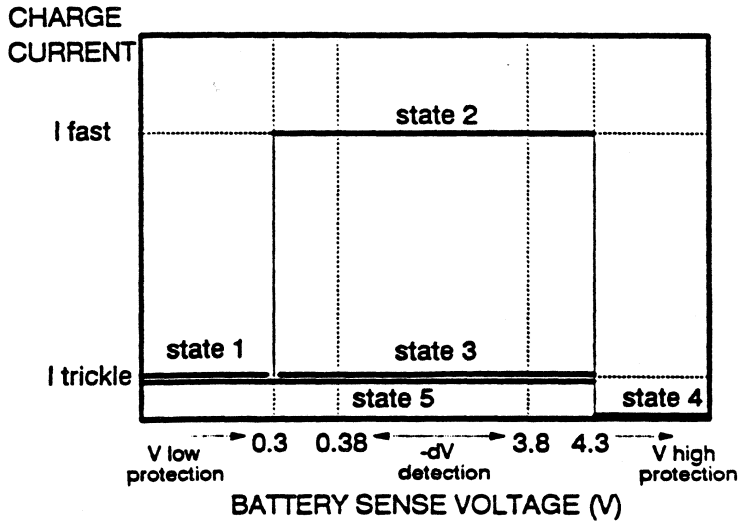


FIG.2 CHARGE STATE DIAGRAM



Operational states of charger system

state 1: Trickle charge with flat battery
state 2: Fast charge
state 3: Trickle charge, battery full detected
state 4: Disabled charge, open circuit shutdown
state 5: Trickle charge with out of range battery temperature

Fig.4 TEA1100 SUPPLY CHARACTERISTIC

(excluding IC source load currents)

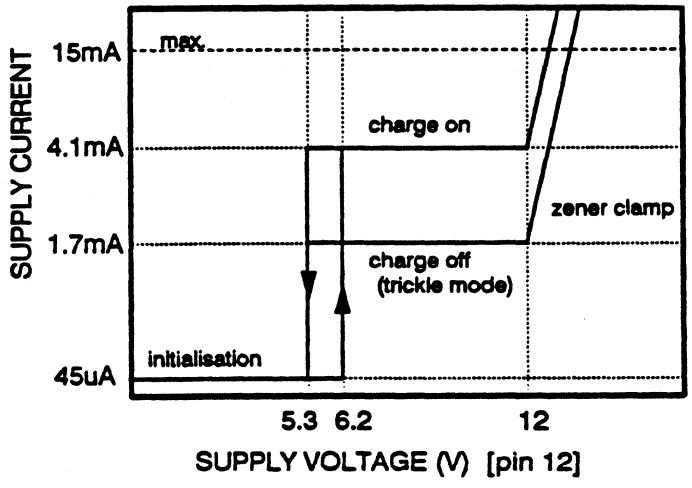
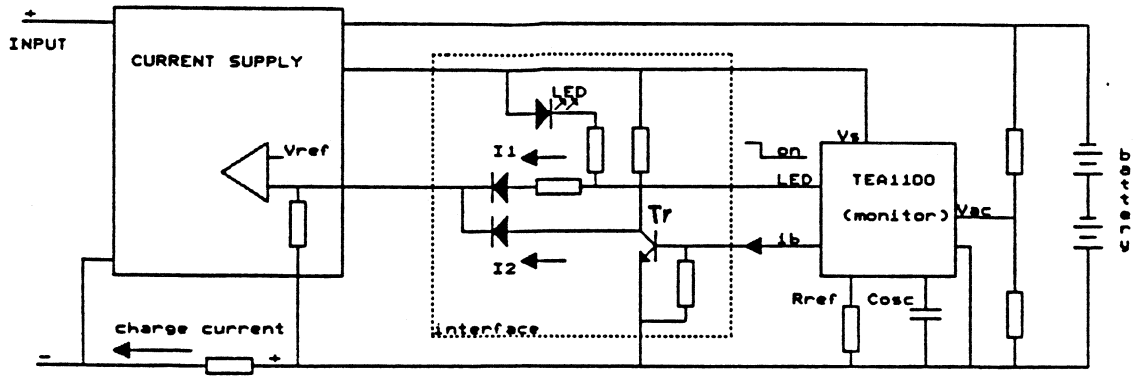


FIG.5 STAND ALONE CHARGER WITH TEA1100



This charger example shows TEA1100 as monitor only, which remotely controls the charge output current from a stand alone SMPS.
The SMPS regulates the charge current by refering to a positive going current sense voltage. Via an interface TEA1100 controls the release of charge current and reduces the trickle charge current magnitude.
This 3 state charge control is realised as follows;

Fast charge: LED output low, ib= i_{Rref} switching Tr on.
Both i1 and i2 currents are zero therefore not affecting the SMPS current sense voltage and the charge is maximum.

Trickle charge burst period:
LED output low, ib= iRref/2 switching Tr off.
i1 current is zero but i2 flows which causes a voltage step on top of the current reference voltage so the charge current magnitude is reduced.

Charge-off period (trickle charge and protection modes):
LED output high, ib= zero.
Both i1 and i2 currents flow. The sum of these currents causes a voltage step which exceeds the comparators' Vref so charge current is disabled.

FIG.6 CHARGE CURRENT REGULATION

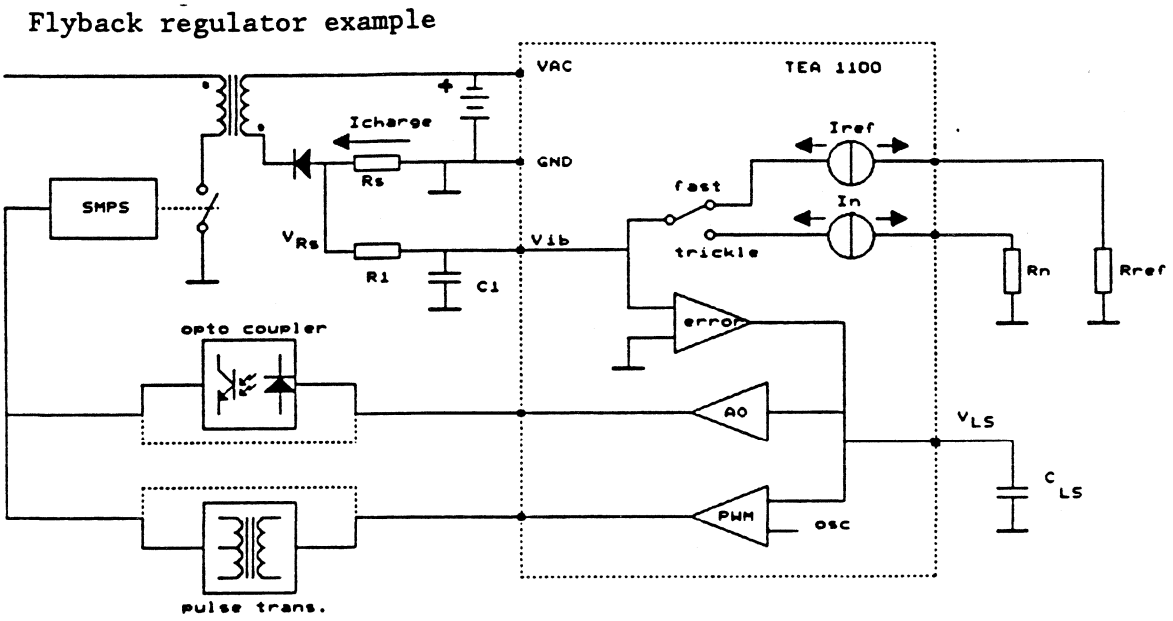


Fig.7 Waveforms related to fig.6

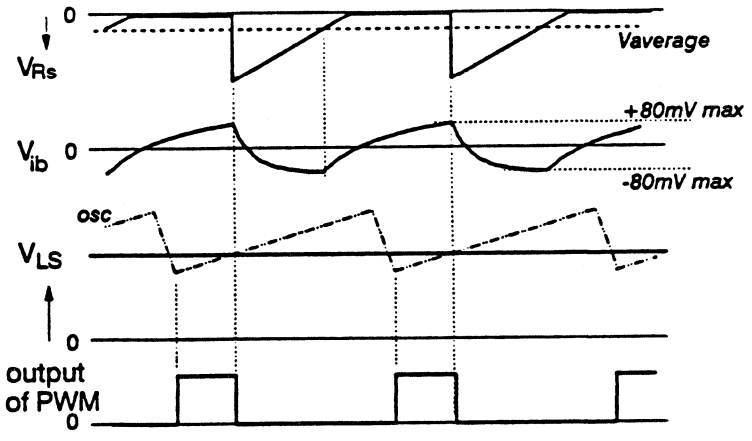


Fig.8 TRANSCONDUCTANCE ERROR AMP

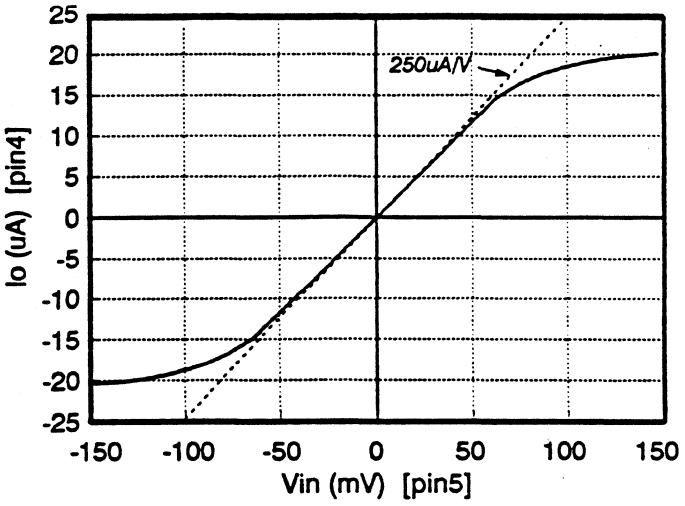


Fig.9 GAIN/PHASE RESPONSE ERROR AMP

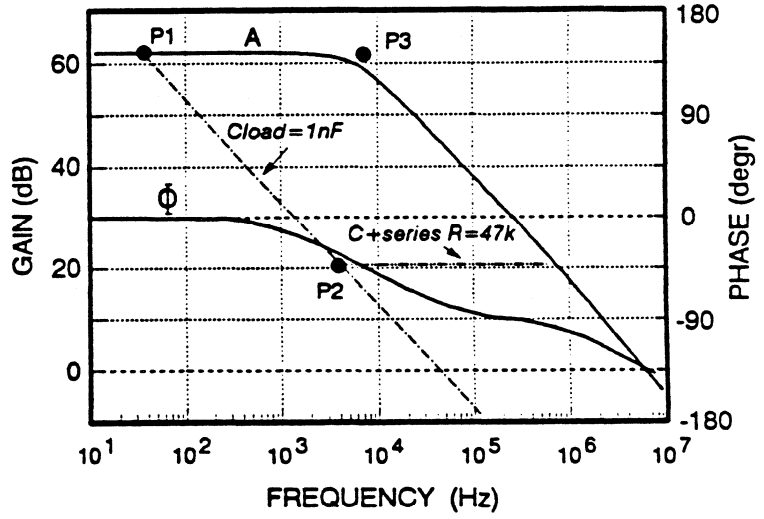


TABLE 2 LOOP COMPENSATION NETWORKS AND RESPONSE

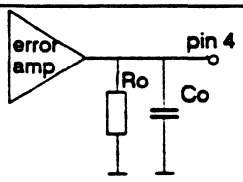
	ac small signal model	with load at LS, pin 4	
	g_M=250µA/V Ro =4.5MΩ Co =4.7pF 		
gain	$A_{(f)} = g_M \frac{Ro}{1+sRoCo}$	$A_{(f)} = g_M \frac{Ro}{1+sRoC}$	$A_{(f)} = g_M (R+\frac{1}{sC})$
poles	$f_3 = \frac{1}{2\pi RoCo} = 8kHz$	$f_1 = \frac{1}{2\pi RoC}$	$f_1 = \frac{1}{2\pi RoC}$
zeros	-	-	$f_2 = \frac{1}{2\pi RC}$

FIG.10 PWM CONTROL AT START-UP

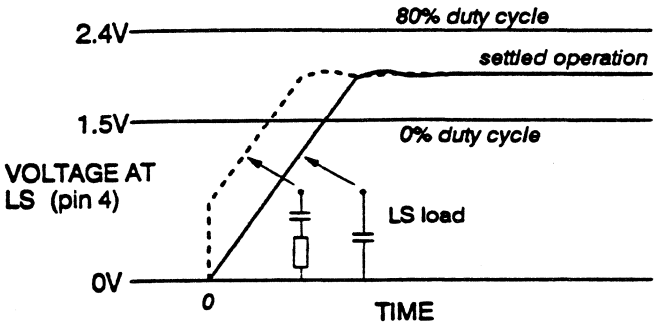


FIG.11 ANALOG AMP TRANSFER CHARACTERISTICS

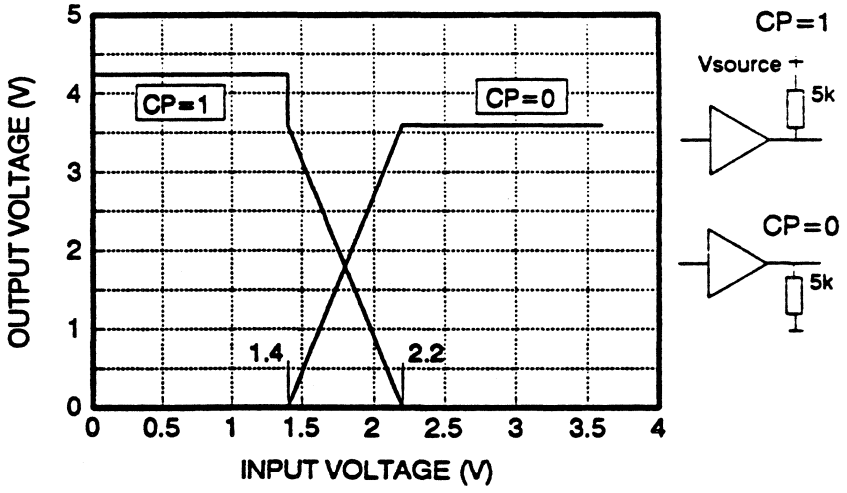


FIG.12 PULSE WIDTH MODULATION

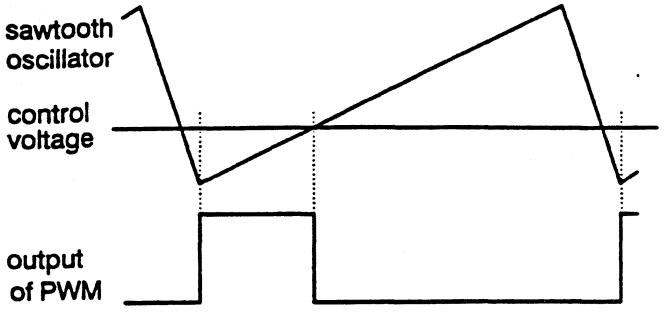


FIG.13 FEED FORWARD CONTROL (flyback SMPS)

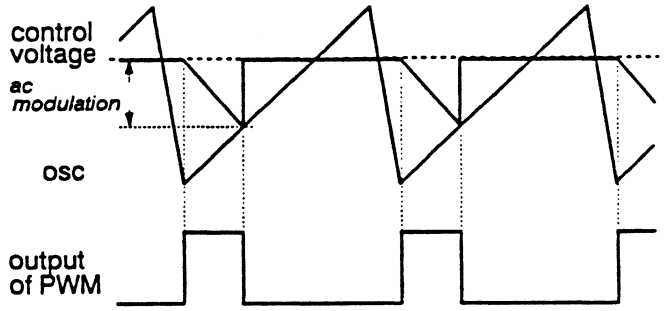
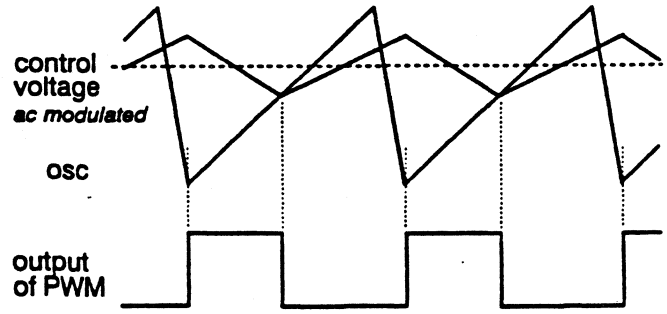


FIG.14 FEED FORWARD CONTROL (forward SMPS)



OPERATIONAL CONDITIONS;

Vin = 10- 16.5V Fast charge current = 1.1A Time out = 56min.
Vout= 0- 6.8V Trickle charge current= 28mA Frequency= 40kHz.

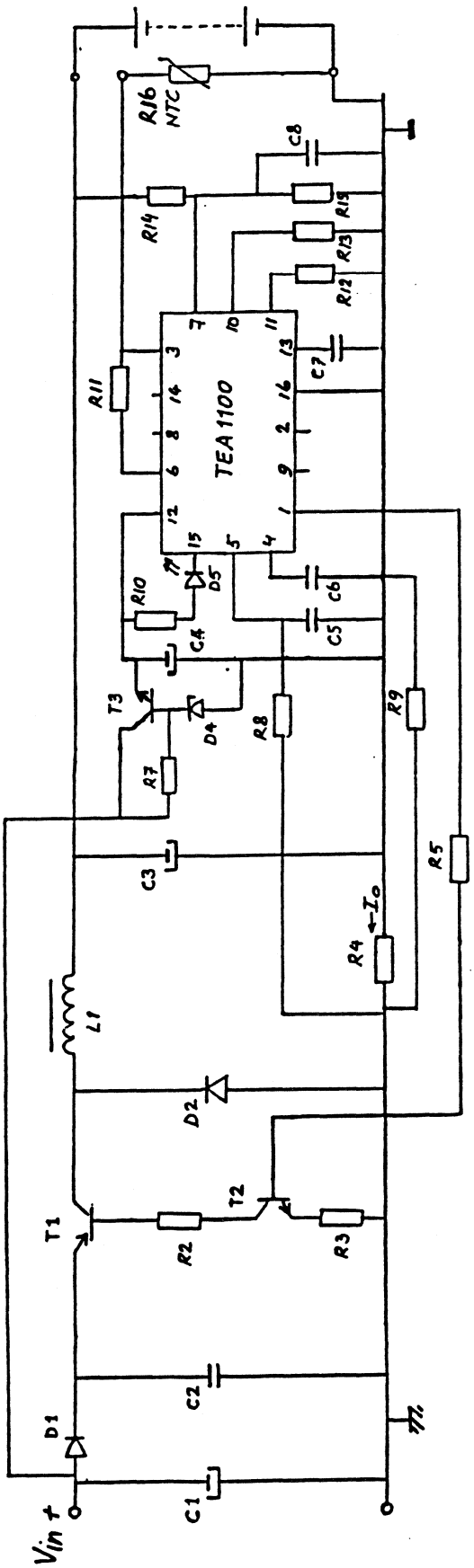


FIG.15 CIRCUIT DIAGRAM OF 12V INPUT, DC/DC CHARGER

TABLE 3. PARTS LIST OF DC/DC CHARGER

Resistors

R1= 330Ω	SFR16T	2322 180 73331
R2= 110Ω	SFR16T	2322 180 73111
R5,R10= 680Ω	SFR16T	2322 180 73629
R4= 4x 1Ω parallel	MRS25 1%	2322 156 11008
R7= 5k1	SFR16T	2322 180 73512
R8= 6k19	MRS25 1%	2322 156 16192
R9= 47k	SFR16T	2322 180 73473
R11= t.b.f.	SFR16T	
R12 not applied		
R13= 27k4	MRS25 1%	2322 156 12743
R14,R15= 27k	SFR16T	2322 180 73273

R16= NTC. If NTC not used then omit R11 and connect pin 3 to pin 11.

Capacitors

C1= 47μF/25V		2222 030 26479
C2= 47nF	MKT 10%	2222 370 11473
C3= 10μF/16V		2222 134 55109
C4= 22μF/16V		2222 134 65229
C5= 82pF	CERAMIC	2222 652 58829
C6,C8= 680pF	CERAMIC	2222 630 08681
C7= 1nF	KP 1%	2222 426 41002

Semiconductors

T1= BD227	9331 603 50127
T2= BC337	9331 492 00000
T3= BC548B	9331 977 60112
D1,D2= BYD73A	9337 537 40153
D4= BZX79 C9V1	9331 177 80000
D5= LED	9338 501 20112

Choke

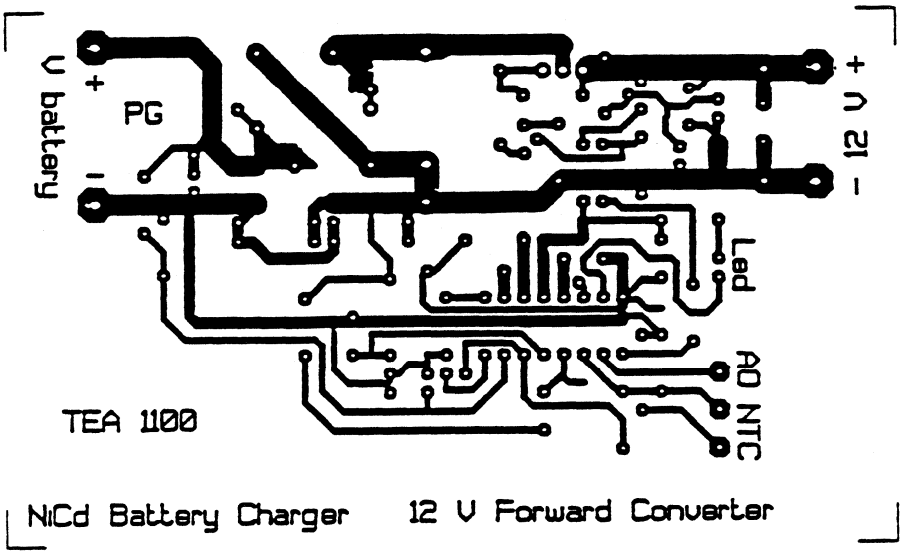
L= 400μH;	
N=50, 0.35mm wire (AWG27)	
RM7/i core set (Al=160)	4322 025 00451
Coil former	4322 021 34611
Clips 2x	4313 021 03951

Miscellaneous

IC 16pins socket	2422 549 13266
Heatsink	2422 487 89039
Pins 4x	

FIG.17 PCB LAYOUT OF THE DC/DC CHARGER

A) PCB COPPER SIDE



B) PCB COMPONENTS SIDE

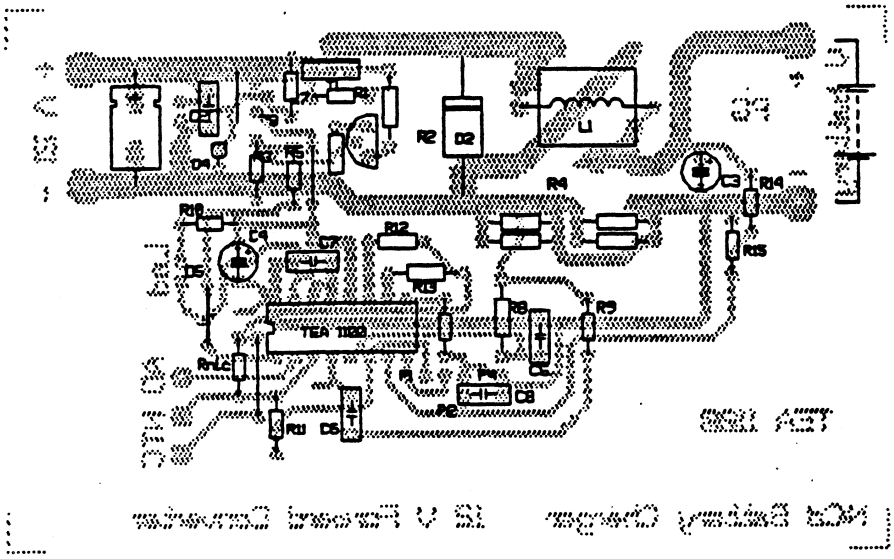
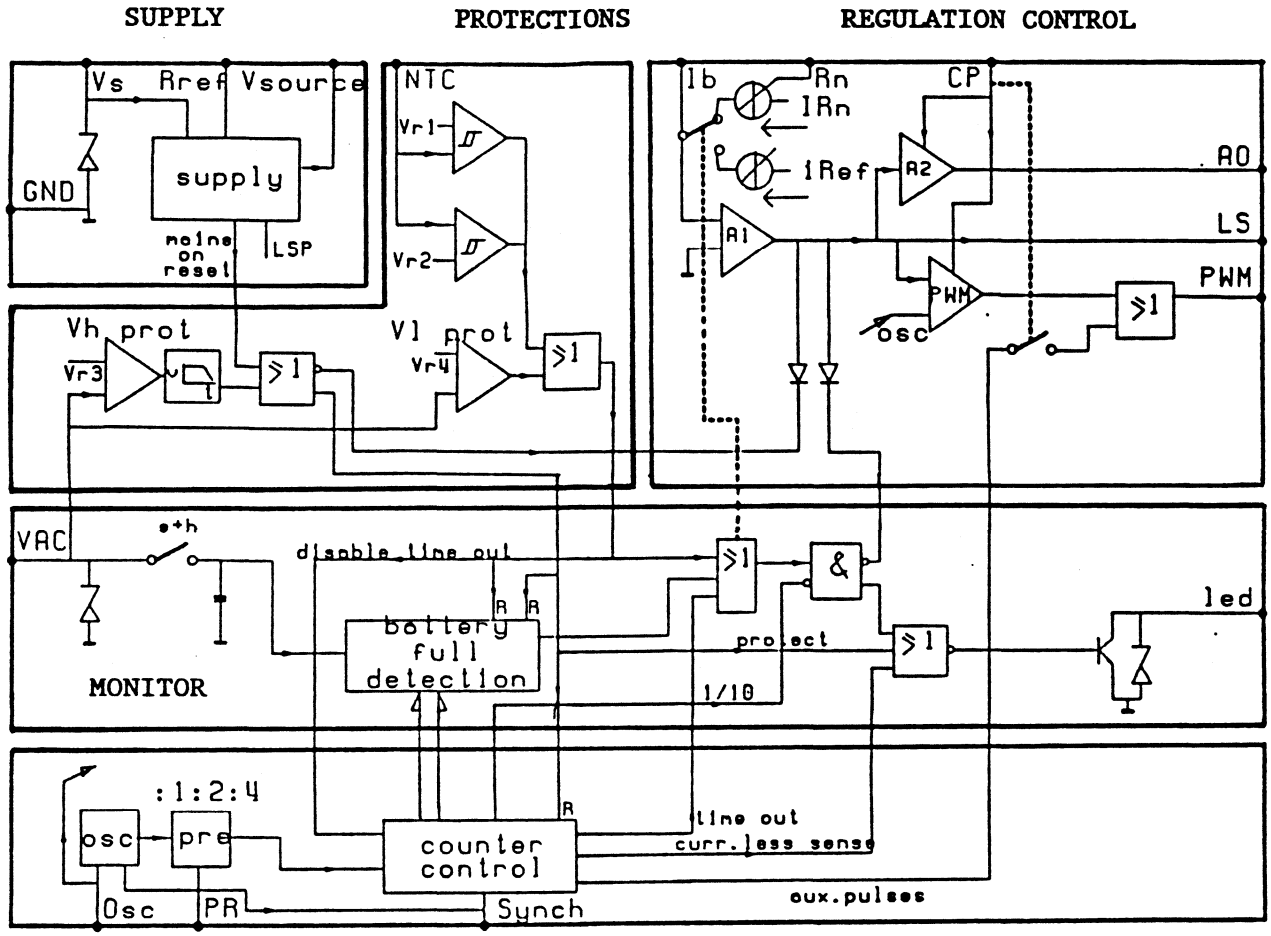
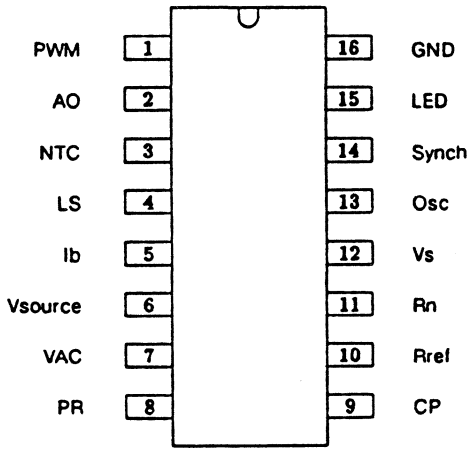
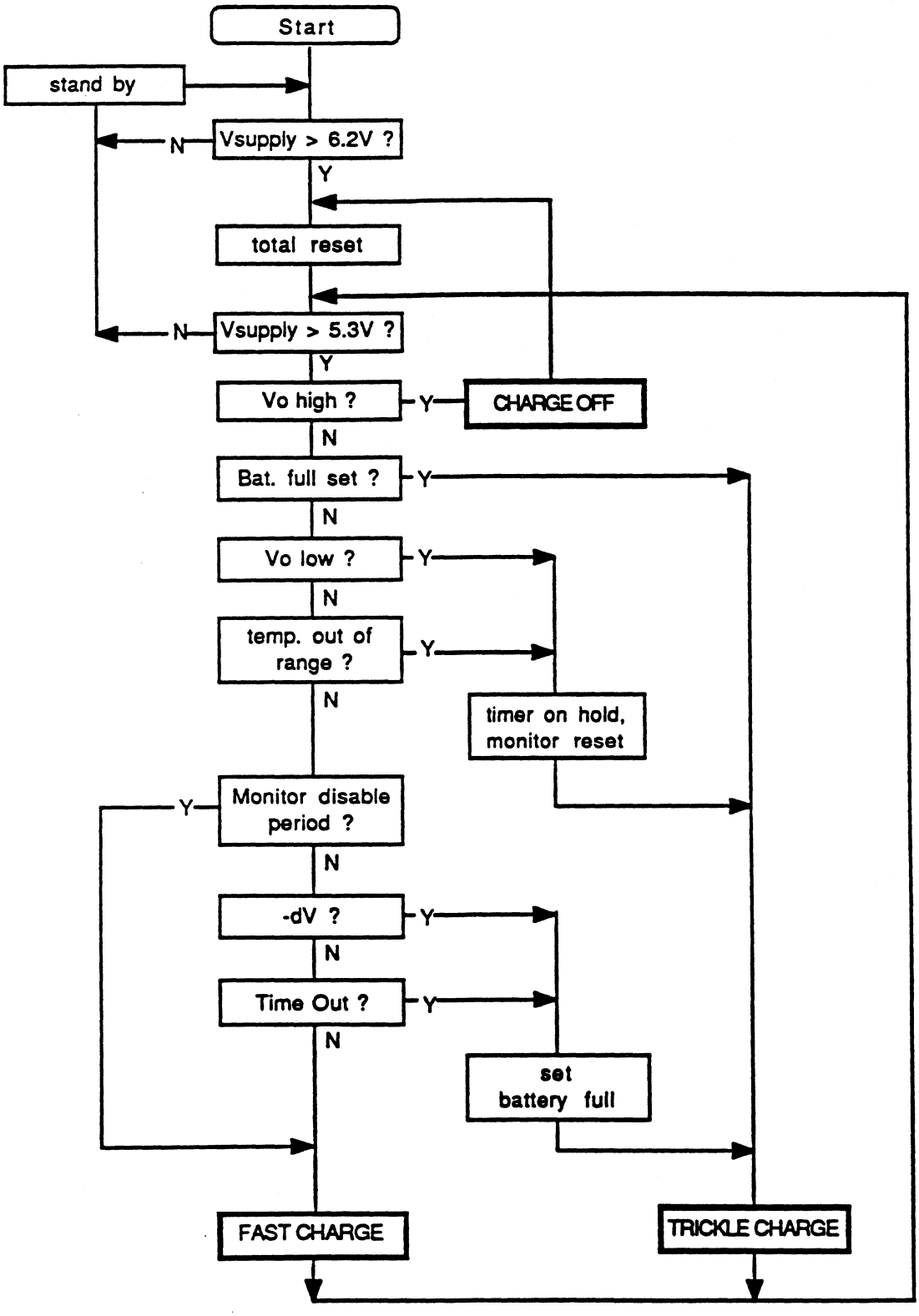


FIG.3 TEA1100 INTERNAL BLOCK DIAGRAM AND PIN CONFIGURATION





Pin number	Function	Description
1	PWM	Pulse Width Modulator
2	AO	Analog Output
3	NTC	Temp sense input
4	LS	Loop Stability
5	Ib	Charge current
6	Vsource	Stabilized supply voltage
7	VAC	Battery voltage
8	PR	Prescaler
9	CP	Change Polarity
10	Rref	Reference resistor
11	Rn	Normal charge ref resistor
12	Vs	Supply voltage
13	Osc	Oscillator
14	Synch	Synchronization
15	LED	LED output
16	GND	Ground



TEA1100 charger flow diagram

APPENDIX 2

APPLICATION NOTE

Method to increase -dV sensitivity for TEA1100 charge system.

The basic design of a high performance battery charge system with TEA1100 features battery full detection by -dV sensing; -1% of the battery top voltage level. This corresponds to a -dV of approximately 16mV per cell. The performance and sensitivity of the -dV detection is broadly accepted as well suited to the task.
In some applications (NiMH or "heavy-duty" NiCd) however an increased sensitivity of -dV detection to -0.5% is required. Although the -1% threshold in TEA1100 is fixed, it is possible to have detection at -0.5% by addition of a zener diode in the battery voltage sense line.
This method is outlined as follows;

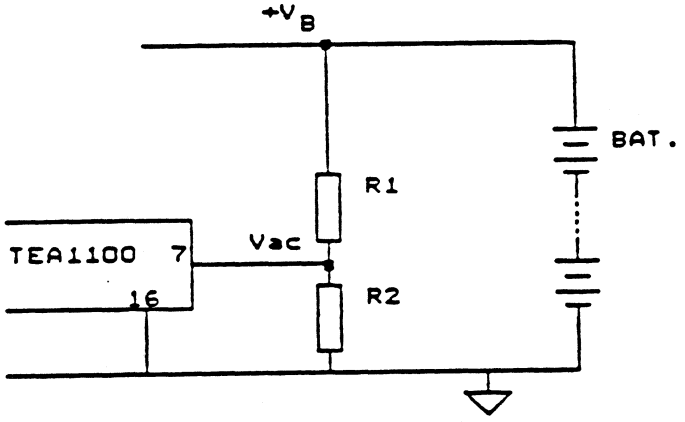


Figure 1

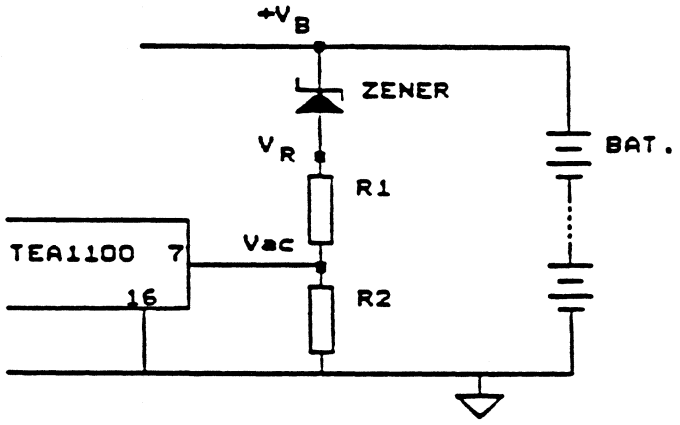


Figure 2

Figure 1 shows the basic, direct battery sensing via a resistive divider which adapts the battery voltage to within the Vac range. Detection occurs at -dV= 1% of V_B max.

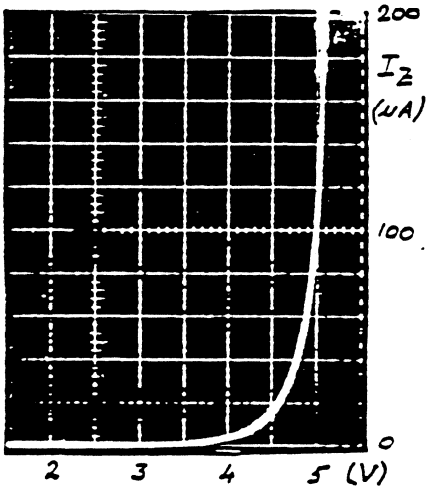
Figure 2 shows the position of the zener diode. TEA1100 now senses the voltage V_R which is the battery voltage minus the zener voltage, V_B - V_R.
Detection occurs at -dV_R= 1% of V_R max. This detection corresponds with a -dV in the battery according to:

$$. dV_B = \frac{V_Z}{V_B \text{ max}} - 1 = \quad (\%).$$

If the zener voltage is half the maximum battery voltage then dV_B detection will be at -0.5%.

The current flowing in the V_{AC} sense network should be small to prevent unwanted high discharge of the battery when the charge supply is switched off. A rule of thumb is that the discharge allowed falls in the range of the battery self discharge rate which is approximate -25% per month. Hence, the equivalent average discharge current for different battery capacity is than;

Battery capacity	**0.5**	**1**	**1.5**	**(AHr)**
Self discharge current	**180**	**360**	**540**	**(μA)**



At these low currents common zeners show a soft knee characteristic which is not applicable. Instead good results are obtained with the Philips low voltage avalanche diode type, the PLVA400A series, specially intended for low current use with tight tolerance. The available voltage range is 5 to 6.8V.

Figure 3 shows the zener characteristic of the 5V diode, PLVA450A.

Design example for a six cells' battery and 0.5% -dV cutoff.

Conditions:	Maximum battery voltage (1.7V/cell)	= 10.2V.
	Sense network current	≈ 300μA.
	Maximum monitor sense voltage V_{AC}	= 3.6V. (<3.85V).

For -dV ≈ 0.5% a zener voltage of about half the battery voltage is required; take V_Z = 5V. Now V_R top level is ≈ 5.2V and the divider factor, V_{AC}/V_R, needed is 0.69. R1 and R2 become respectively 5.6kΩ and 12kΩ.

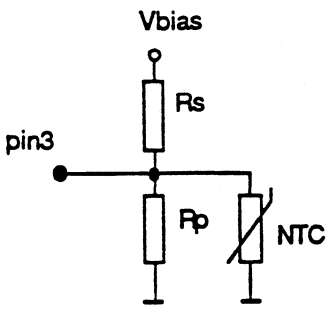
During charge the battery voltage rises with a minimum rate of about 8mV per minute for 6 cells under 1C charge. The temp. coefficient of the zener and its ambient temperature change should not cause a premature full detection.
With the following equation the allowance of zener temperature change can be derived;

$$\frac{K}{min} < \frac{0.5\%(V_B - V_Z) + 8mV/min}{S_Z}$$

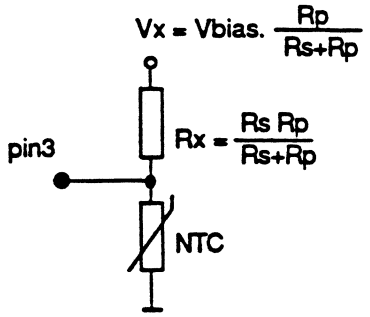
At the early stage of charge V_B is ≈ 8.4V for 6 cells, 0.5% is a safe figure for 1% detection in TEA1100 and V_Z = 5V.
If assumed a S_Z = +0.5mV/K (typ. 0.2mV/K for PLVA450A) then the outcome is 50°K/min maximum.

Appendix 3

Battery NTC thermistor adaption to TEA1100 temperature sense input.



Temperature sense network



Equivalent circuit

For the low and high temperature levels the corresponding R_h and R_l thermistor resistance values needs to be derived

The following calculations is a way to get the values of the required battery serie-, parallel resistor and the bias voltage;

low temperature limit , NTC resistance :	R_h	ratio; $p = \frac{R_h}{R_l}$
high temperature limit, NTC resistance :	R_l	
TEA1100 upper threshold	Vh = 3V	range; $\Delta V_t = 2.19V$
lower threshold	Vl = 0.81V	

If $k = \frac{\Delta V_t}{(p \cdot V_l) - V_h}$ then $\quad Rx = k \cdot R_h \;;\; Vx = V_h(1+k)$

V_B = constant bias voltage ; $\quad Rs(eries) = \frac{k}{3(1+k)} \cdot V_B \cdot R_h$

($V_B \geq Vx$) $\quad Rp(arallel) = \frac{k}{V_B - 3(1+k)} \cdot V_B \cdot R_h$

When the B value of the NTC is used then ; $\quad p = e^{B \cdot \left(\frac{1}{Tl} - \frac{1}{Th}\right)}$ T is in Kelvin.

$$R_h = R_{25} \cdot e^{B \cdot \left(\frac{1}{Tl} - \frac{1}{298}\right)}$$

Note: Without temperature sensing pin 3 can directly be connected to pin 11.

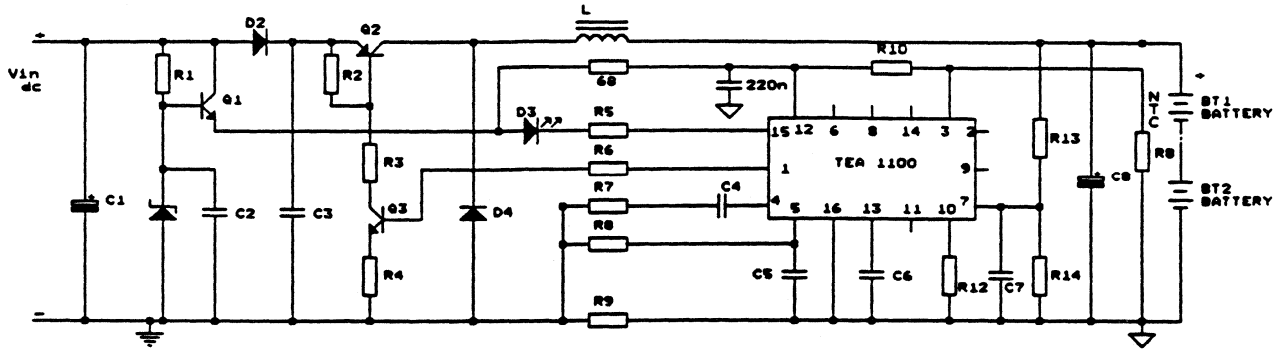


FIG. IV-a. CHARGER DIAGRAM WITH BIPOLAR SWITCH IN THE BUCK REGULATOR

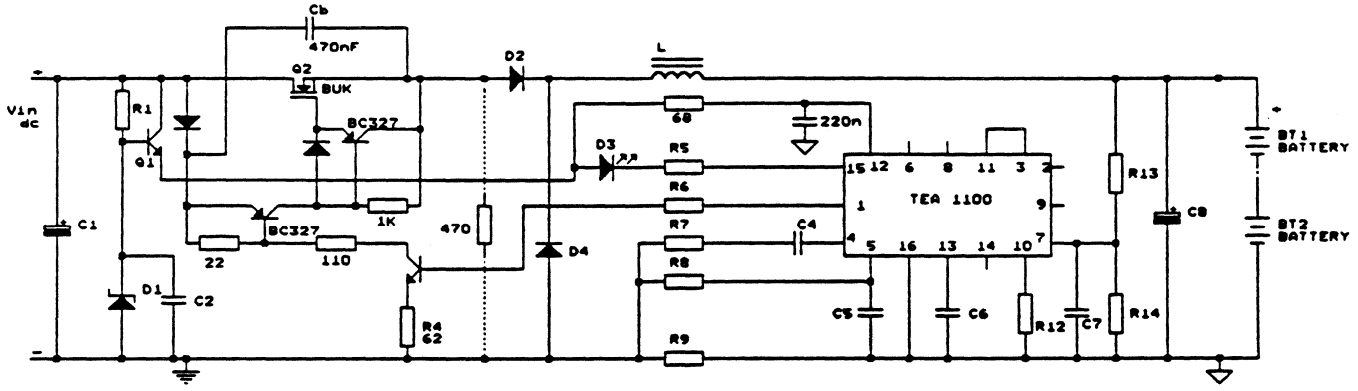


FIG. IV-b. CHARGER DIAGRAM WITH N CHANNEL POWERMOSFET SWITCH IN THE BUCK REGULATOR

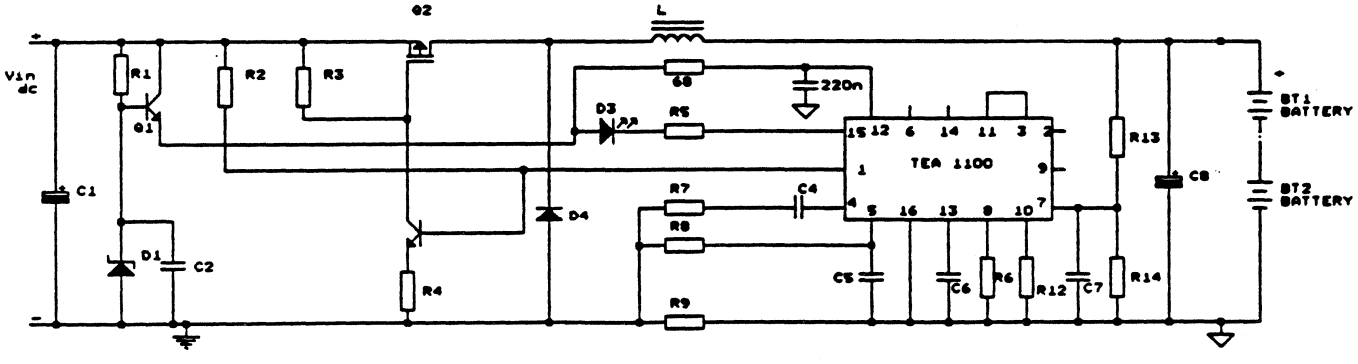


FIG. IV-c. CHARGER DIAGRAM WITH P CHANNEL POWERMOSFET SWITCH IN THE BUCK REGULATOR

Appendix 4-2

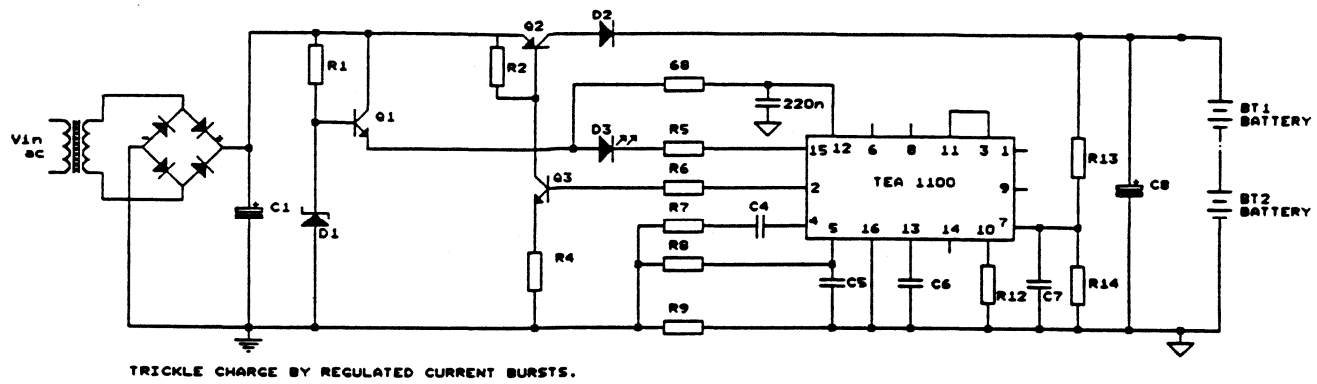


FIG. 4d CHARGER DIAGRAM WITH DIRECT CURRENT SERIES REGULATION.

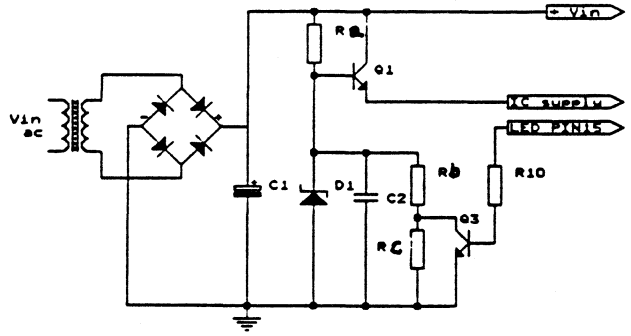
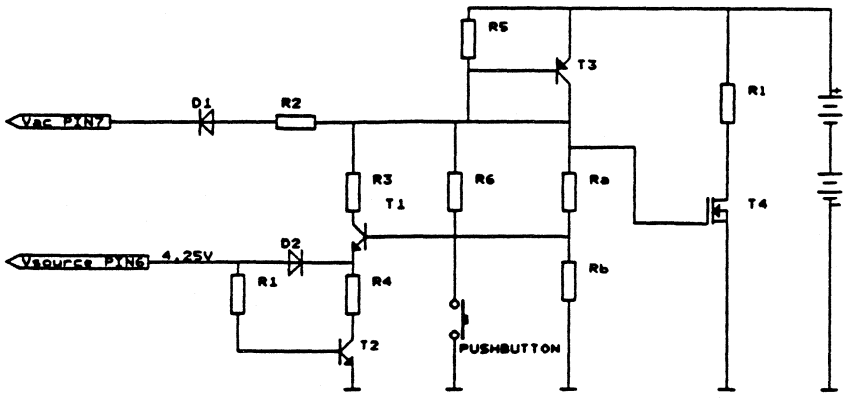


FIG. 4e SYSTEM OPERATION WITH SUPPLY HYSTERESIS CONTROL

When charge current starts flowing and internal resistance in the system input supply causes a noticeable voltage dip, then charger on/off switching can occur; this can be prevented by using a supply hysteresis control. With the divider Ra over Rb or Ra over Rb and Rc, controlled by Q3 via the LED signal of TEA1100, a large supply hysteresis can be programmed.

Appendix 5



DISCHARGE BEFORE CHARGE EXAMPLE

When the feature, discharge before charge is required, then this circuit can fulfil this option and is applicable for a 5 or more cell's battery.
Discharge is switched-on on demand by pressing the pushbutton, only when the charger is on. During discharge, charge is disabled by forcing the Vac high into protection and remains so until the batteries' divided voltage by Ra/Rb drops below 4.25V. This terminates the discharge latch function and restarts the charge sequence.
Instead of the discharge power Mosfet, a bipolar power transistor is an alternative.

Transistor functions;

T2: enables latching,T1 and T3, when TEA1100 is on.
T1: comparator within the latch.
T3: latch driver switch for T4 and Vac high setting via D1.